

## Application Performance: Altix vs. the Rest

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## Agenda

- RRZE
- Altix Basics
  - Architecture
  - Software
  - Competitors
- Applications
  - CFD
    - SIP Solver (OpenMP)
  - Physics
    - DMRG (SCSL)
    - DMRG (OpenMP)
- Conclusions



## **RRZE Machine Structure**



- 8 CPUs @ 2.2 GFlops, 2 GB
- Installed 1997
- SGI Origin 3400
  - 28 CPUs @ 500 MHz (R14k)
  - 56 GB
  - Installed June 2001
- IA32 Cluster
  - 86x2 Xeon 2.66 GHz
  - Gigabit Ethernet
  - Installed April 2003
- **SGI Altix 3700** 
  - 28 CPUs @ 1.3 GHz
  - 112 GB
  - Installed December 2003
- Several test systems
  - Opteron, Xeon, IT1, IT2



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Altix Performance



## **Altix Basics**





## Altix Software



## **Altix Competitors**

- IBM p690
  - 32-CPU ccNUMA
  - dual Core Power4
- NEC TX7
  - 32-CPU ccNUMA, Itanium 2
  - 4 CPUs per memory path
- NEC SX6
  - Vector CPU, 0.5 words/flop
  - Shared memory node with 8 CPUs, full bandwidth
- Intel Xeon systems
  - IA32 architecture, high clock rates
- AMD Opteron systems
  - X86-64 architecture, enhancements over IA32
  - one path to memory per CPU
  - 8-CPU SMPs with hardly any external hardware



## **CFD: Strongly Implicit Solver (SIP)**





SIP-solver



Data dependencies & Implementations
Basic data dependency: (i,j,k)+{(i-1,j,k);(i,j-1,k);(i,j,k-1)}

do k = 2 , kMax do j = 2 , jMaxdo i = 2 , iMax  $RES(i,j,k) = \{ RES(i,j,k) - LB(i,j,k) * RES(i,j,k-1) \}$ - LW(i,j,k)\*RES(i-1,j,k)- LS(i,j,k)\*RES(i,j-1,k) \$ \$ = LP(i,j,k)enddo enddo enddo 3-fold nested loop (3D): (i,j,k) Hyperplane: (i+j+k=const) • Data locality (Caches !) Non-contiguous memory access vectorization of innermost loop No shared memory parallelization (Hitachi: *Pipeline parallel processing*) unsuitable for RISC systems









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#### SIP-solver Pipeline Parallel Processing using OpenMP





### SIPSolver (ppp): NUMA Placement Problems



- Internode communication on Altix is significantly slower than intra-node (factor of 2 worse than Origin)
- Consequence: Data locality is even more important than on Origin
  - "First Touch" policy maps memory pages in the node where they are first used
  - Initialization of data structures must be parallelized to ensure proper placement!





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## DMRG













# DMRG Algorithm





## **DMRG Algorithm**



#### **Implementation**

- Start-Up with infinite-size algorithm
- DM diagonalization: LAPACK (dsyev) costs about 5 %
- Superblock diagonalization costs about 90 % (Davidson algorithm)
- Most time-consuming step: Sparse matrix-vector multiply (MVM) in Davidson (costs about 85 %)
- Sparse matrix *H* is constructed by the transformations of each operator in *H*:

$$H_{ij;i'j'} = \sum_{\alpha} A^{\alpha}_{ii'} B^{\alpha}_{jj'}$$

Contribution from system block and from environment

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#### DMRG Algorithm: Parallelization

#### Implementation of sparse MVM

Sparse MVM: Sum over dense matrix-matrix multiplies!

$$\sum_{i'j'} H_{ij;i'j'} \psi_{i'j'} = \sum_{\alpha} \sum_{i'} A^{\alpha}_{ii'} \sum_{j'} B^{\alpha}_{jj'} \psi_{i'j'}$$

- However A and B may contain only a few nonzero elements, e.g. if conservation laws (quantum numbers) have to be obeyed
- To minimize overhead an additional loop (running over nonzero blocks only) is introduced

$$egin{aligned} H\psi &= \sum_{lpha} \sum_{k} \left( H\psi 
ight)^{lpha}_{L(k)} \ &= \sum_{lpha} \sum_{k} A^{lpha}_{k} \psi_{R(k)} \left[ B^{\mathrm{T}} 
ight]^{lpha}_{k} \end{aligned}$$

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 Dense matrix-matrix multiplies are implemented using DGEMM from BLAS



## **DMRG Serial Performance**







200

## **DMRG: Potential Parallelization approaches**



- 1. Linking with parallel BLAS (DGEMM)
  - Does not require restructuring of code
  - **Significant speedup only for large (transformation) matrices (A, B)**

#### 2. Shared-Memory parallelization of outer loops

- Chose OpenMP for portability reasons
- Requires some restructuring & directives
- Speedup should not depend on size of (transformation) matrices Maximum speedup for total program:
- if MVM (accounts for 85%) is parallelized only: ~6 8

#### **MPI** parallelization

Requires complete restructuring of algorithm -> new code

## **DMRG: Parallel BLAS**





#### **DMRG: OpenMP Parallelization Scalability on Origin** Origin 3400 **OpenMP** scales (Hubbard 4X4, m=2000, half filling) significantly better than parallel DGEMM ideal Aindahl, s=0.02 7 Aindahl, s=0.16 MVM OpenMP 🔺 Davidson OpenMP Serial overnead ... parallel MVM is only and s about 2%! 6 н. Total OpenMP Total DGEMM Linking with parallel н. **BLAS** gives an additional performance gain 6 5 of 15 %! **CPUs**

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## **DMRG Scalability**





Application: Ground State of 21×6 (Open×Periodic) BCs Hubbard ladder with 12 holes





Previously possible only with up to 7x6 sites!

## Parallel DMRG: References





