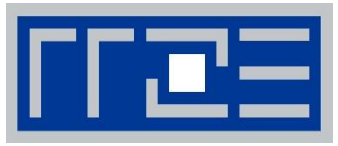


Dr. Georg Hager
Regionales Rechenzentrum Erlangen (RRZE)
Friedrich-Alexander-Universität Erlangen-Nürnberg

Supercomputer

MÄCHTIGES WERKZEUG UND FORSCHUNGSOBJEKT

Fragen

Was ist ein Computer und was kann er?

Was ist ein *Super*computer?

Welche Fragen kann man mit Supercomputern beantworten?

Welche Probleme stellen sich dabei?

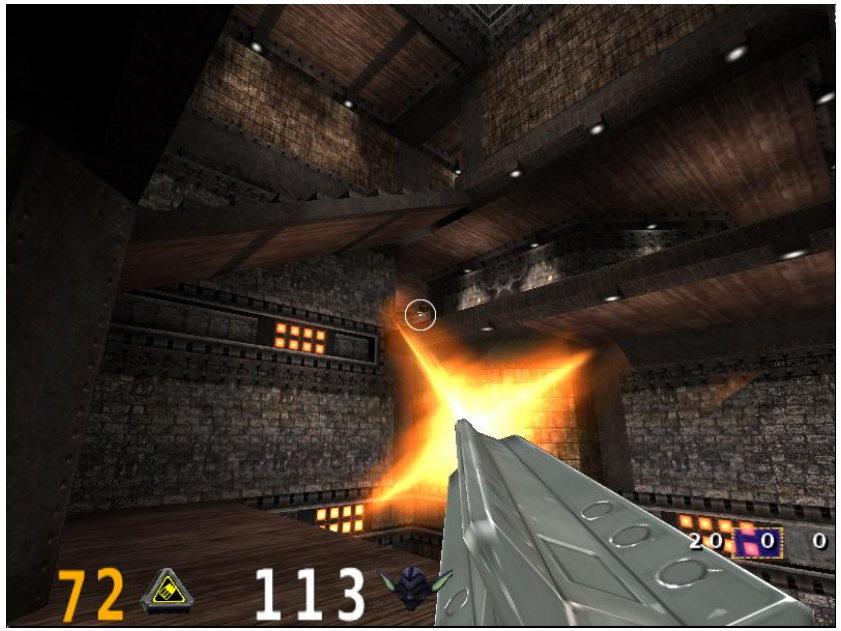
Warum soll ich mich dafür interessieren?

Computer

engl. “to compute” – “rechnen”, “errechnen”, “ausrechnen”

Computer

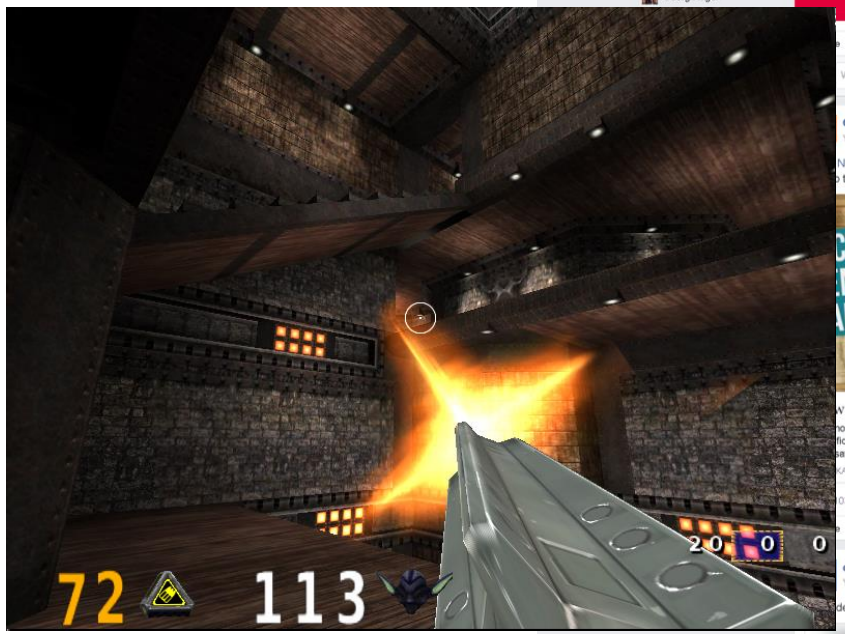
engl. “to compute” – “rechnen”, “errechnen”, “ausrechnen”



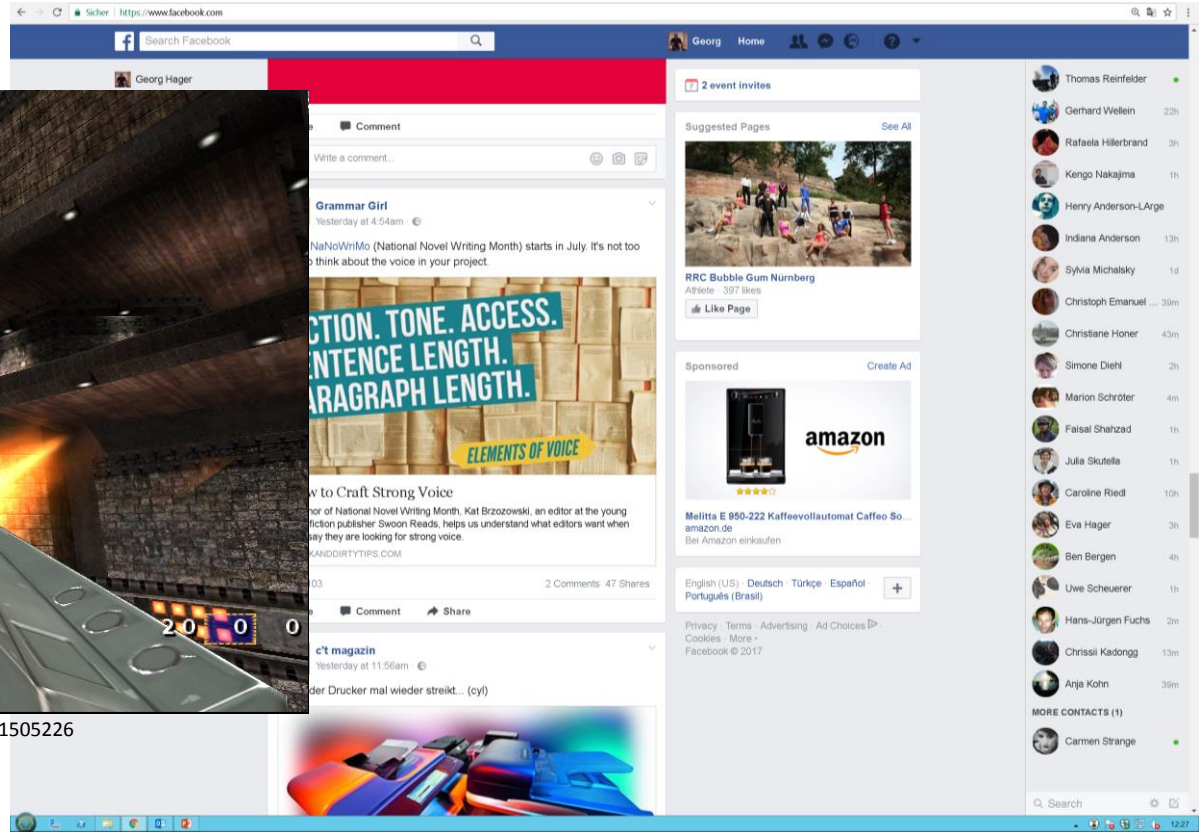
GPL, https://commons.wikimedia.org/w/index.php?curid=1505226

Computer

engl. “to compute” – “rechnen”, “errechnen”, “ausrechnen”

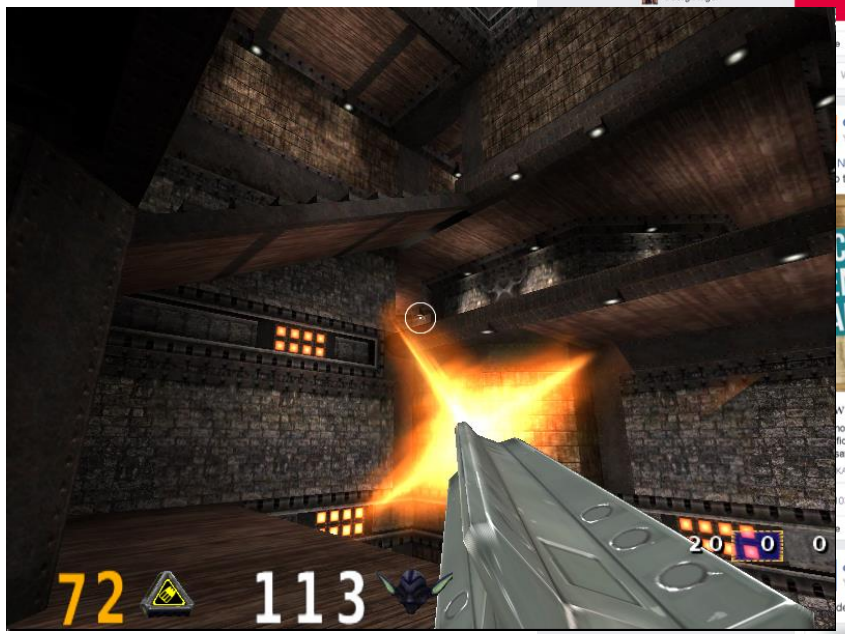


GPL, https://commons.wikimedia.org/w/index.php?curid=1505226

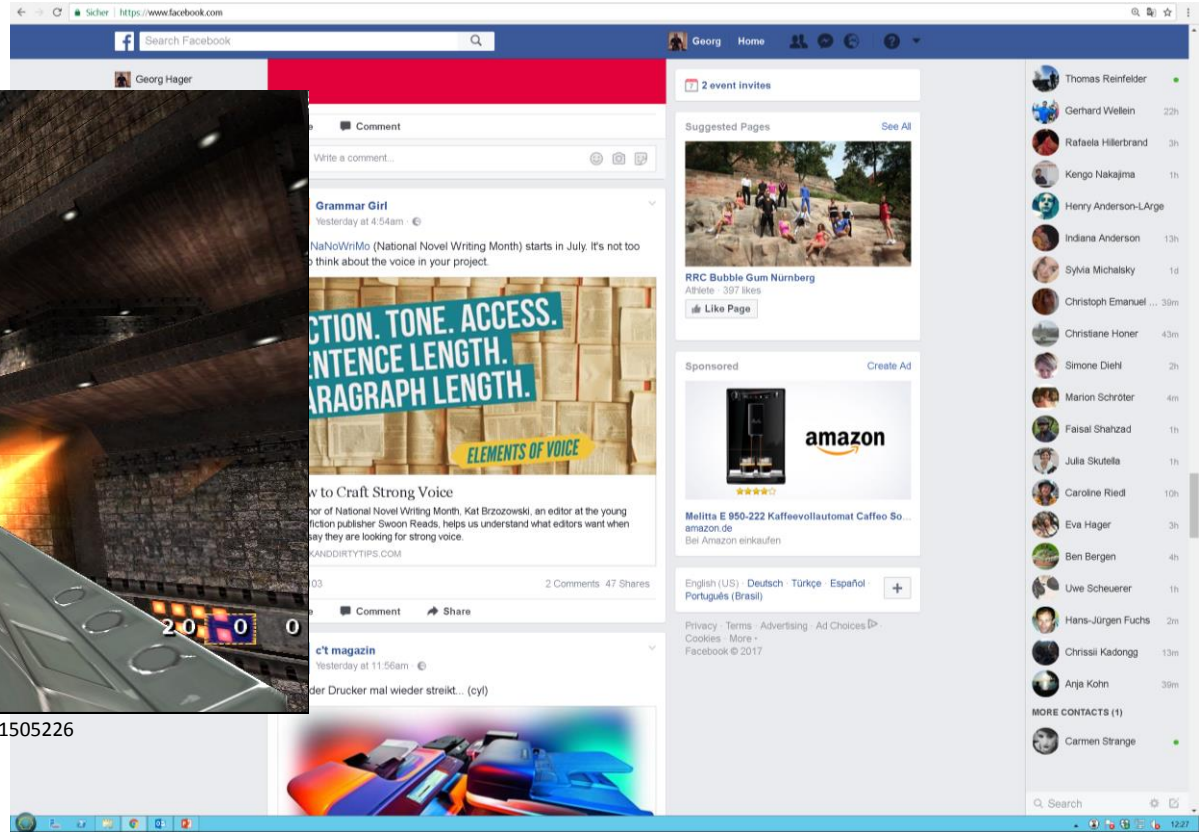


Computer

engl. “to compute” – “rechnen”, “errechnen”, “ausrechnen”



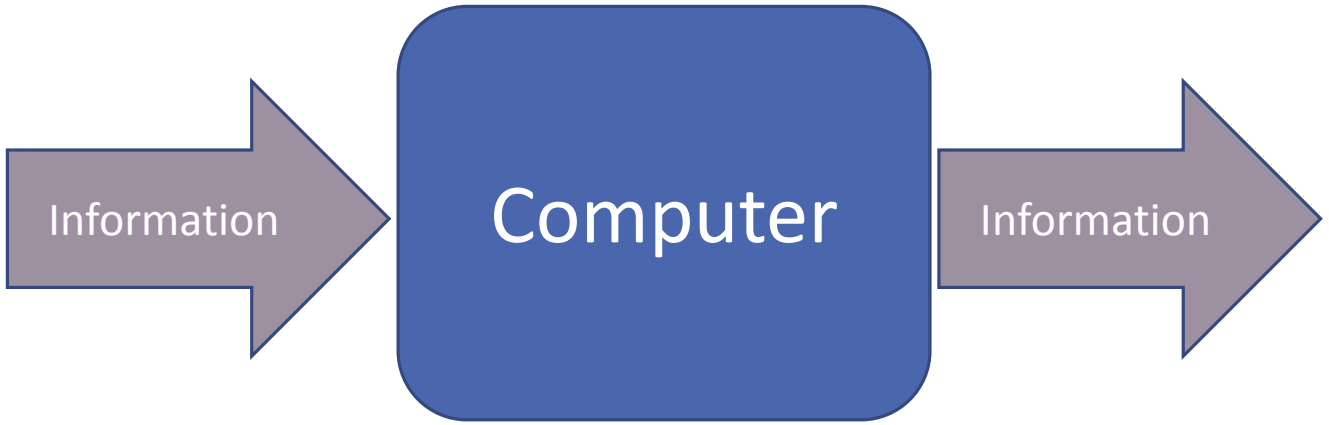
GPL, https://commons.wikimedia.org/w/index.php?curid=1505226



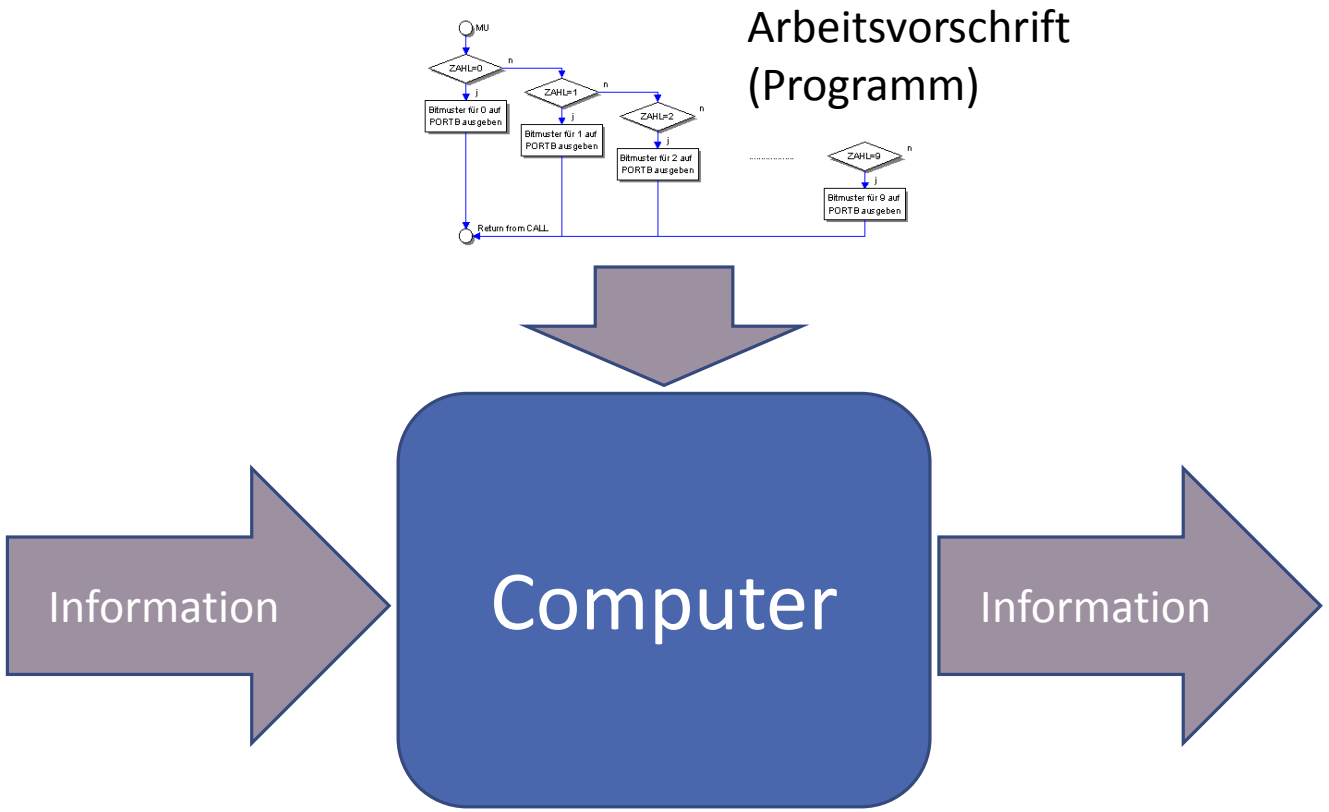
Rechnen.
Aha.

Computer als „großer hohler Raum“

Computer als „großer hohler Raum“

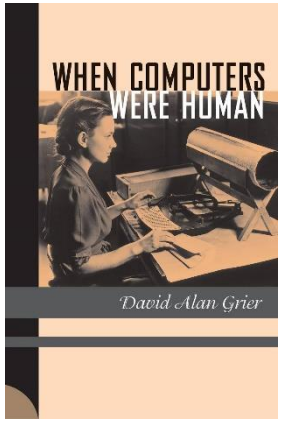


Computer als „großer hohler Raum“

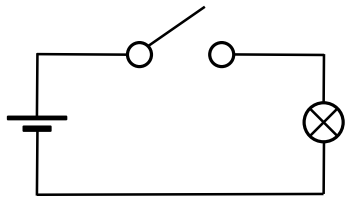


Eine recht allgemeine Definition…

By NACA (NASA) - Dryden Flight Research Center Photo Collection - http://www.dfrc.nasa.gov/Gallery/Photo/Places/HTML/E49-54.html, Public Domain, https://commons.wikimedia.org/w/index.php?curid=885426

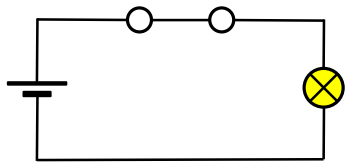


Vom Schalter zum Transistor zum Gatter



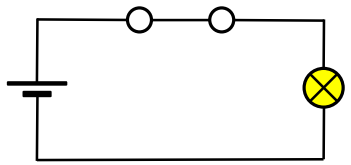
0

Vom Schalter zum Transistor zum Gatter

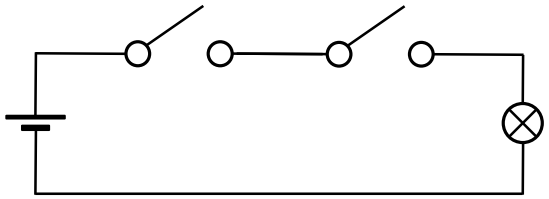


1

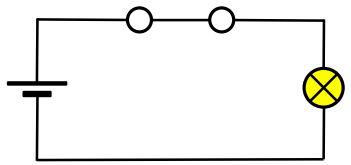
Vom Schalter zum Transistor zum Gatter



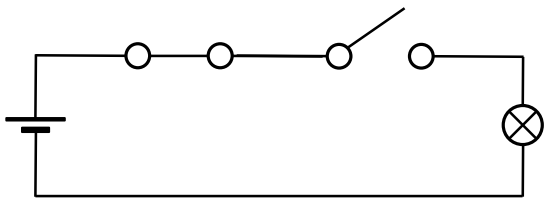
1



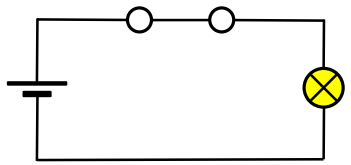
Vom Schalter zum Transistor zum Gatter



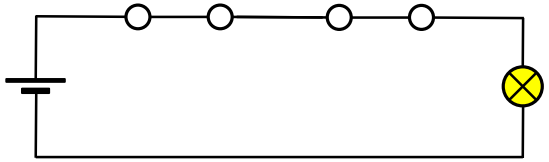
1



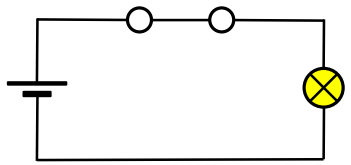
Vom Schalter zum Transistor zum Gatter



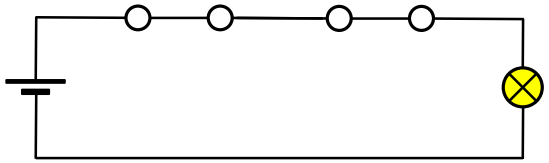
1

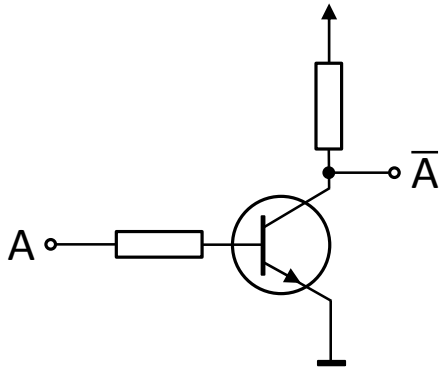


Vom Schalter zum Transistor zum Gatter



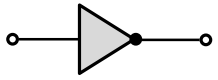
1



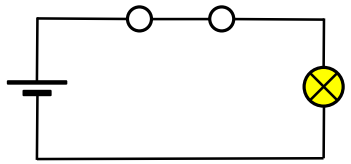


„NOT“

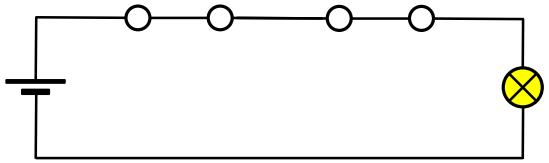
A	$\overline{A}$
0	1
1	0

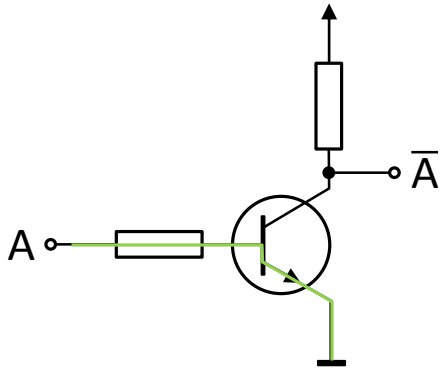


Vom Schalter zum Transistor zum Gatter



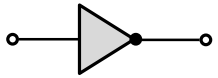
1



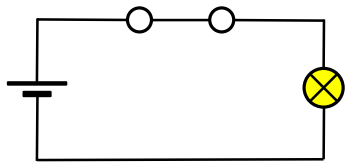


„NOT“

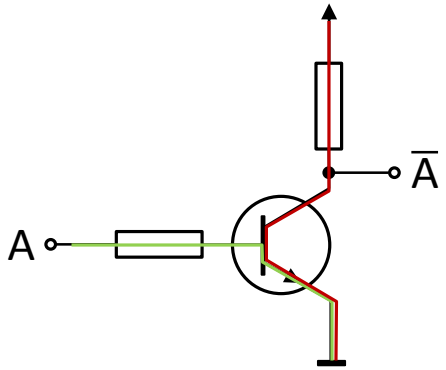
A	$\overline{A}$
0	1
1	0

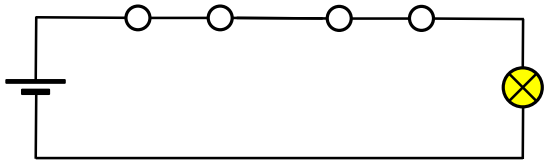


Vom Schalter zum Transistor zum Gatter



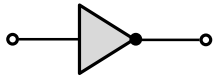
1



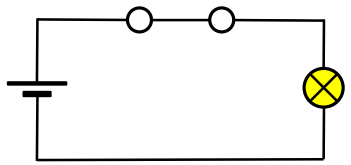


„NOT“

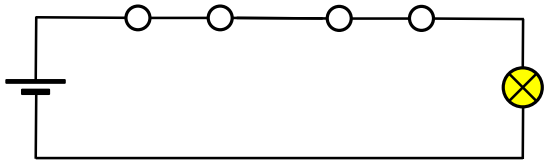
A	$\overline{A}$
0	1
1	0

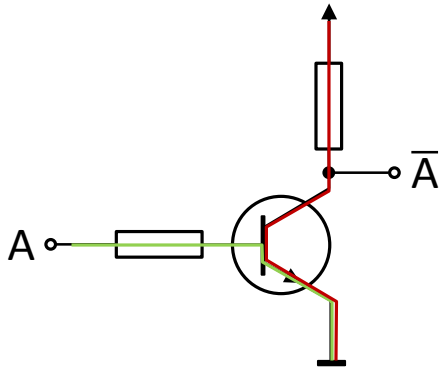


Vom Schalter zum Transistor zum Gatter



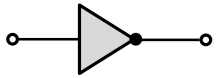
1

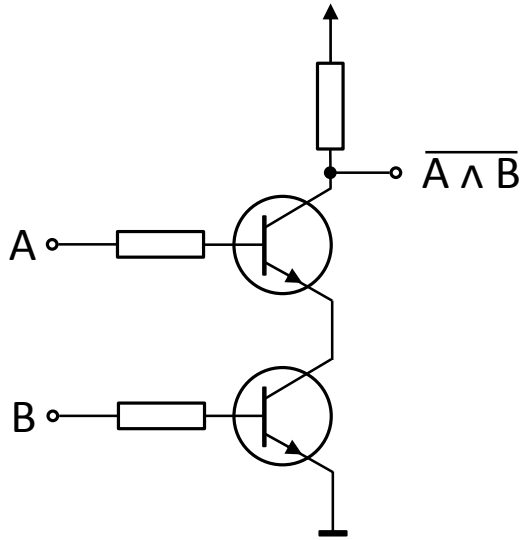




„NOT“

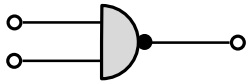
A	$\overline{A}$
0	1
1	0



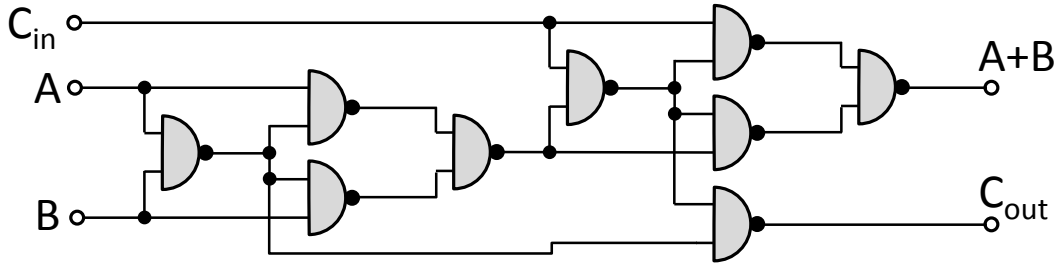


„NAND“

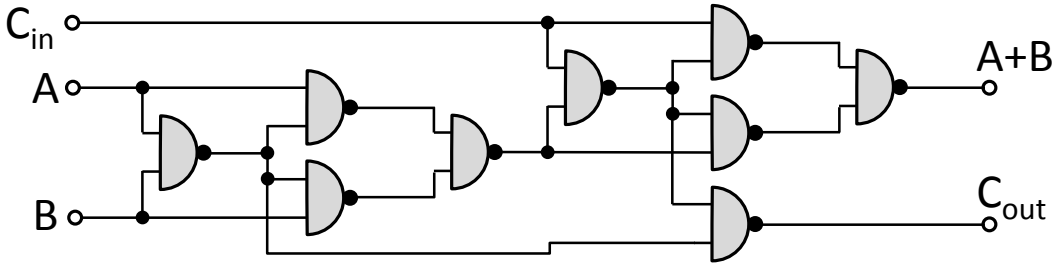
A	B	$\overline{A \wedge B}$
0	0	1
1	0	1
0	1	1
1	1	0



Vom Gatter zum Volladdierer



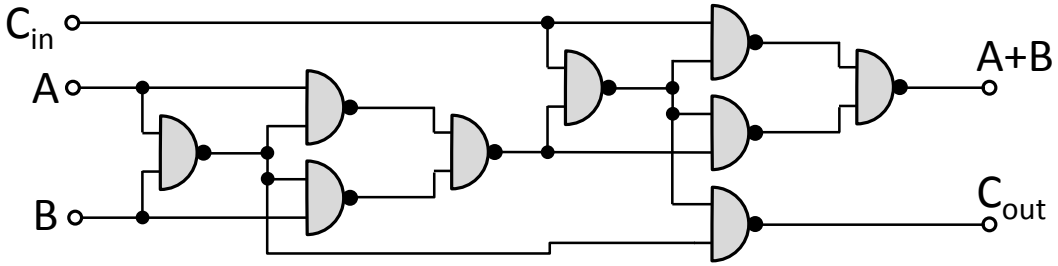
Vom Gatter zum Volladdierer



A	B	C_{in}	A+B	C_{out}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

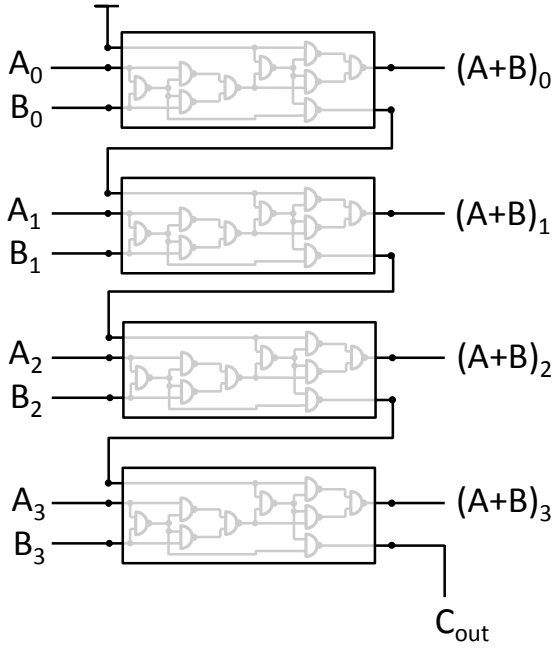
„1-Bit Volladdierer“

Vom Gatter zum Volladdierer



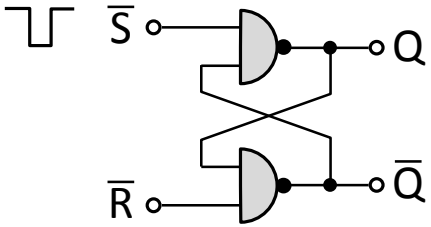
A	B	C_{in}	A+B	C_{out}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

„1-Bit Volladdierer“

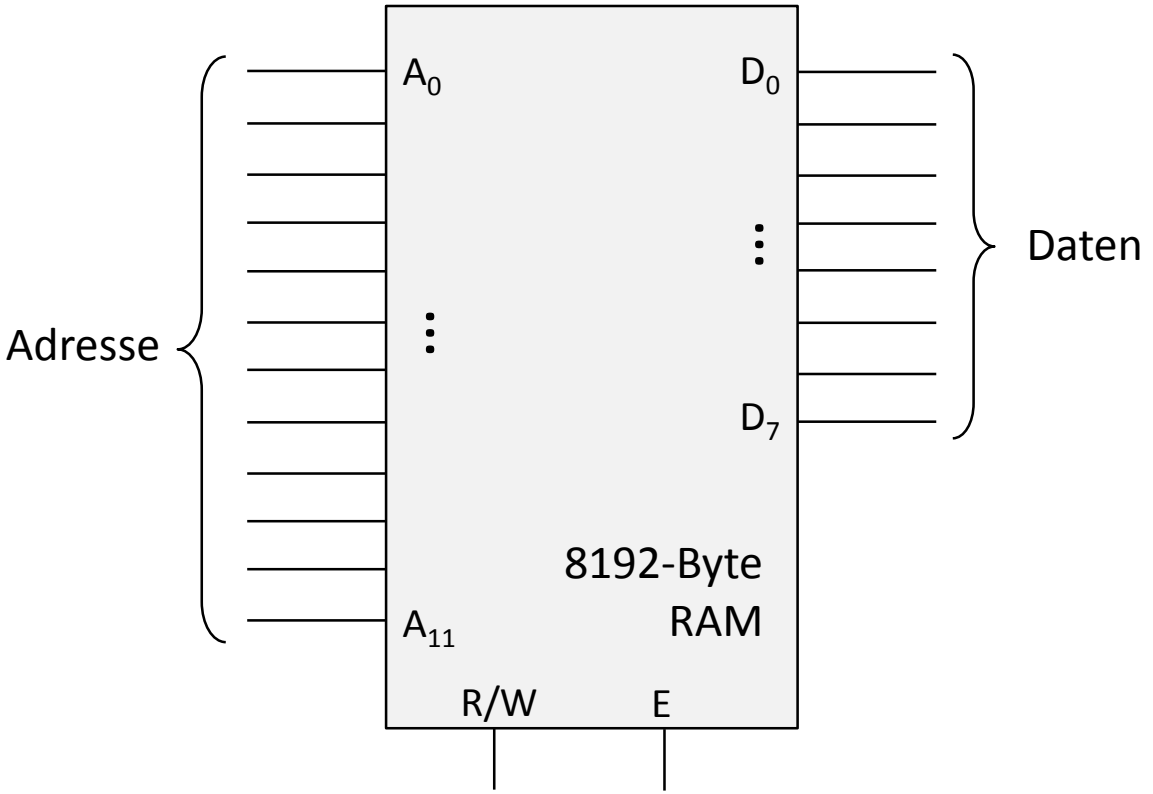


„4-Bit Volladdierer“

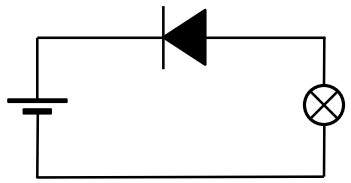
Vom Gatter zum Schreib-Lese-Speicher



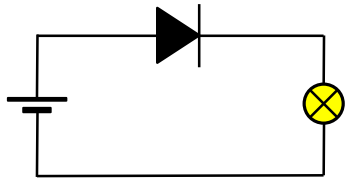
„RS-Flip-flop“
Als 1-Bit-Speicher



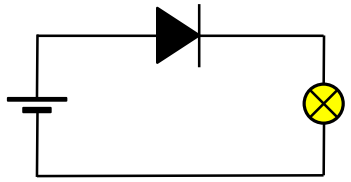
Von der Diode zum Festspeicher

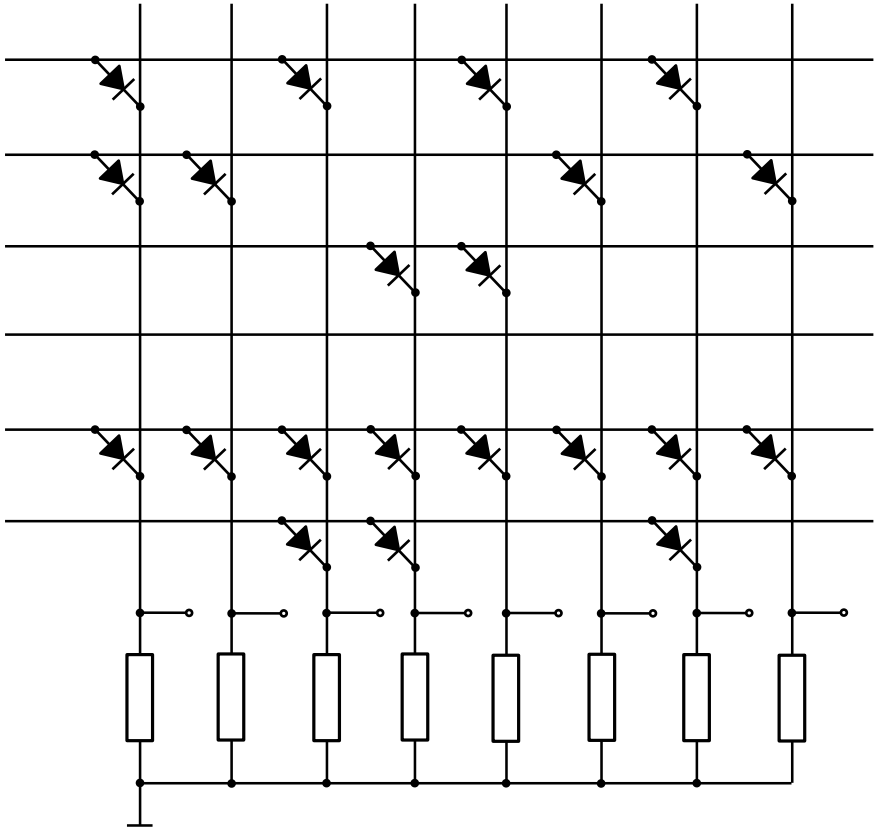


Von der Diode zum Festspeicher

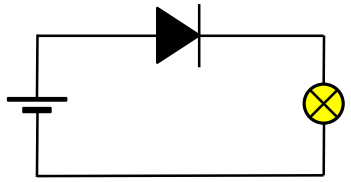


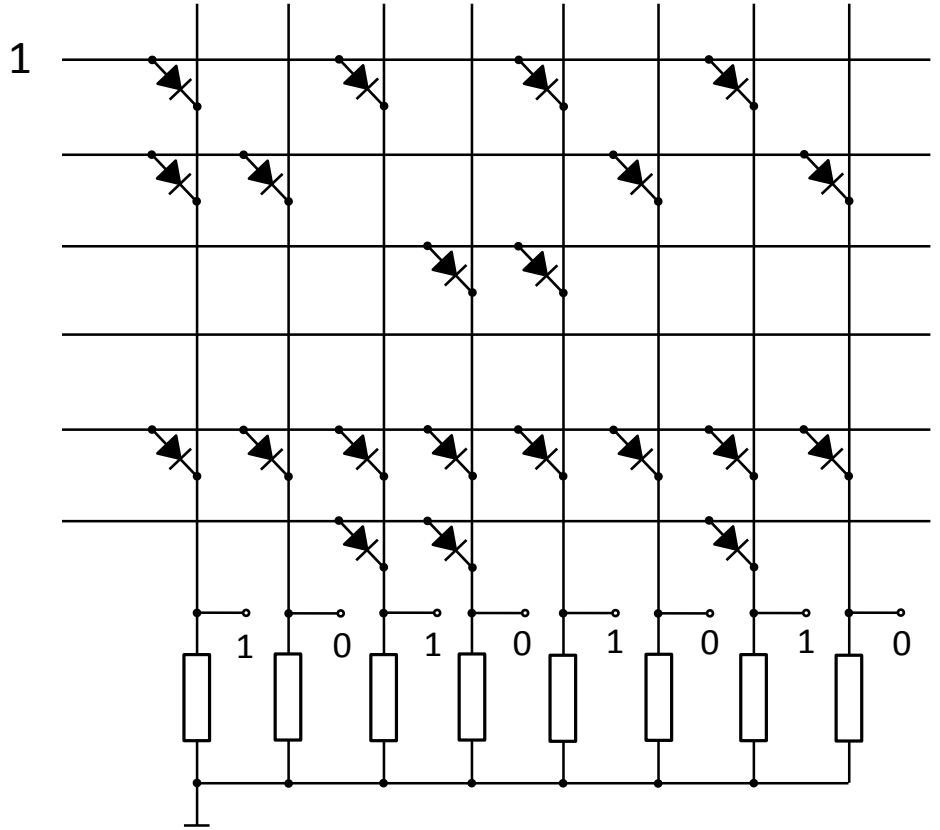
Von der Diode zum Festspeicher



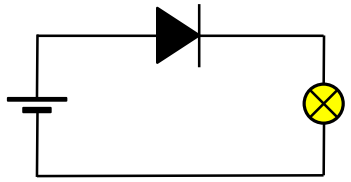


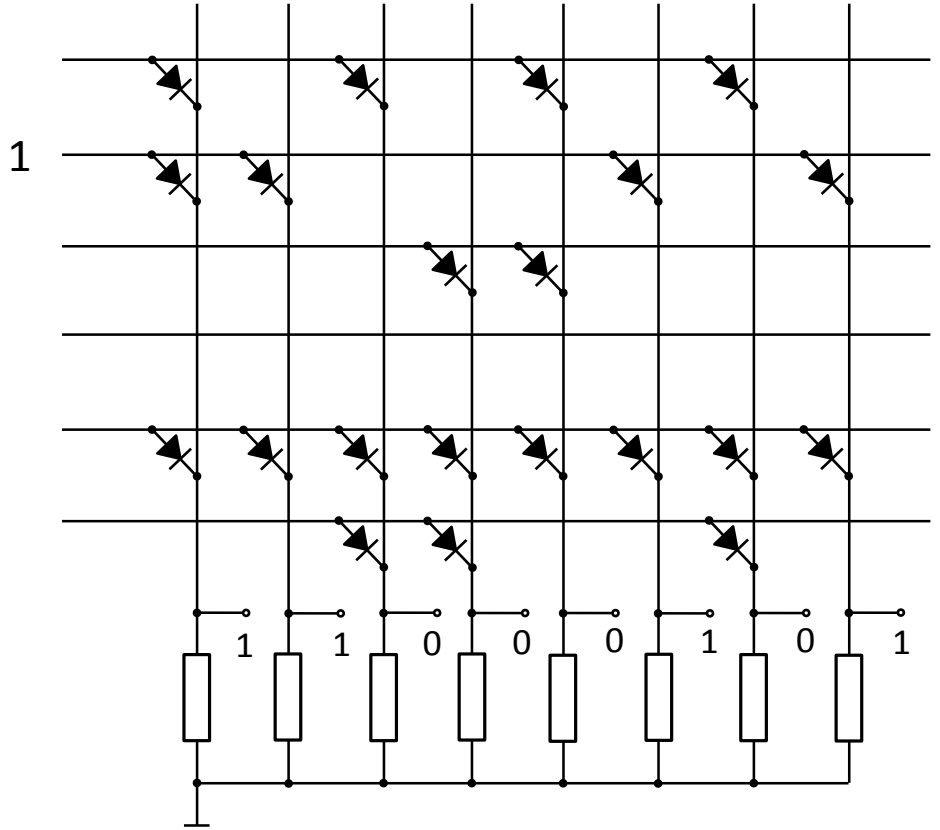
Von der Diode zum Festspeicher



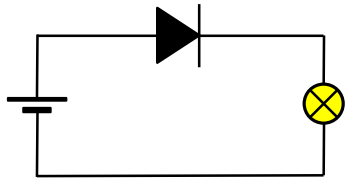


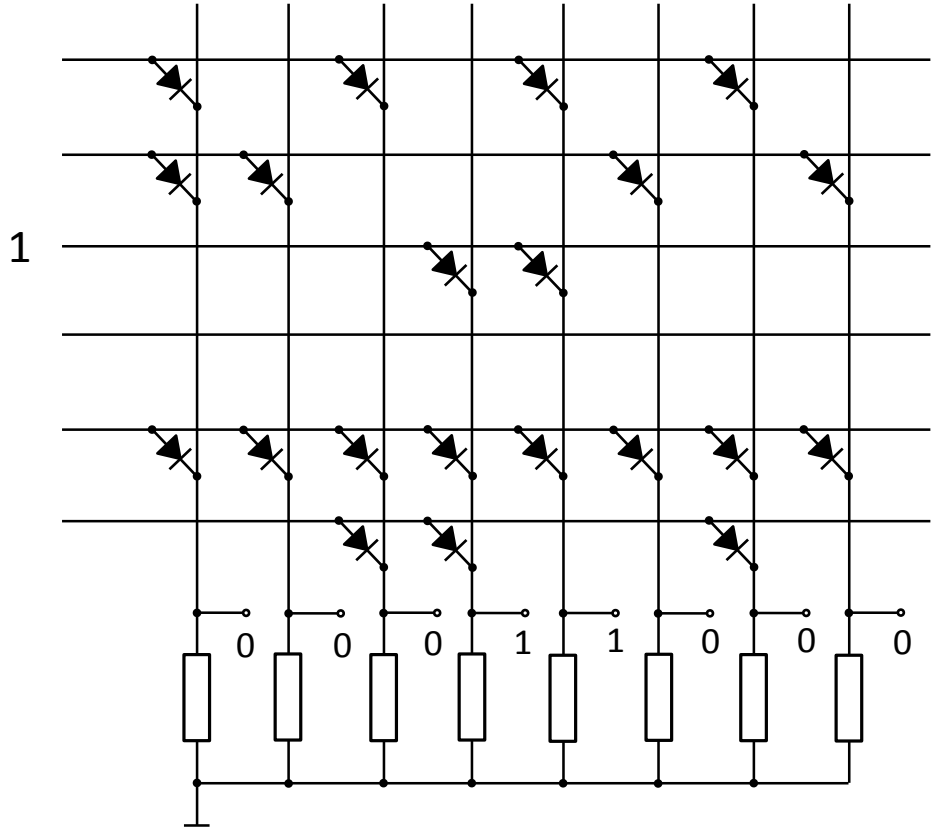
Von der Diode zum Festspeicher



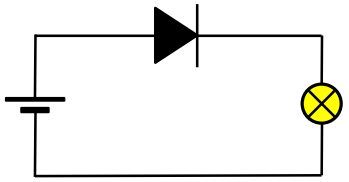


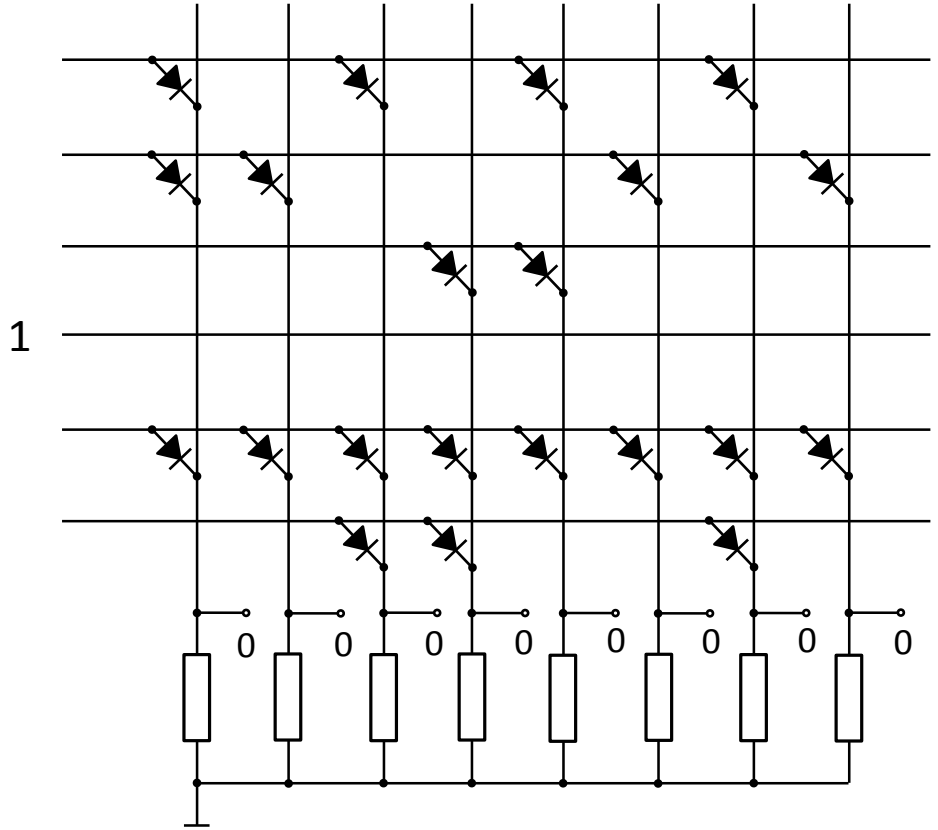
Von der Diode zum Festspeicher



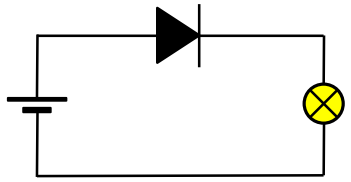


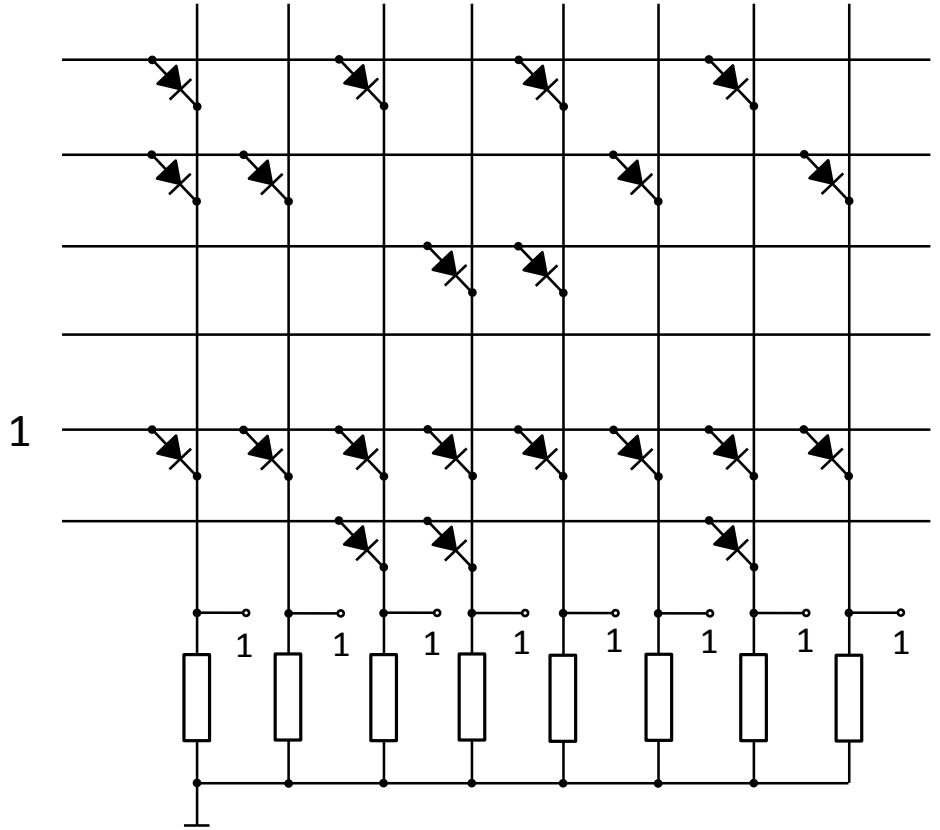
Von der Diode zum Festspeicher



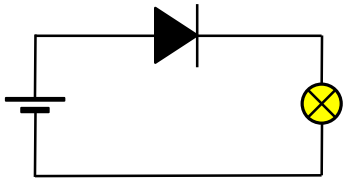


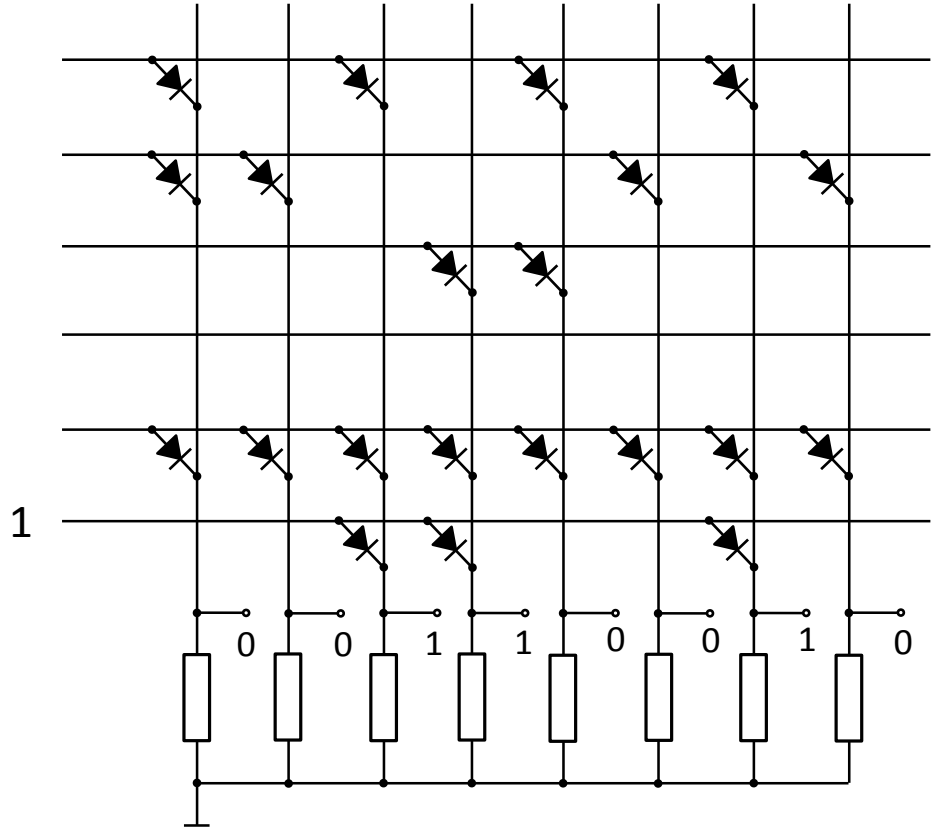
Von der Diode zum Festspeicher



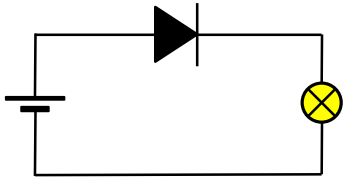


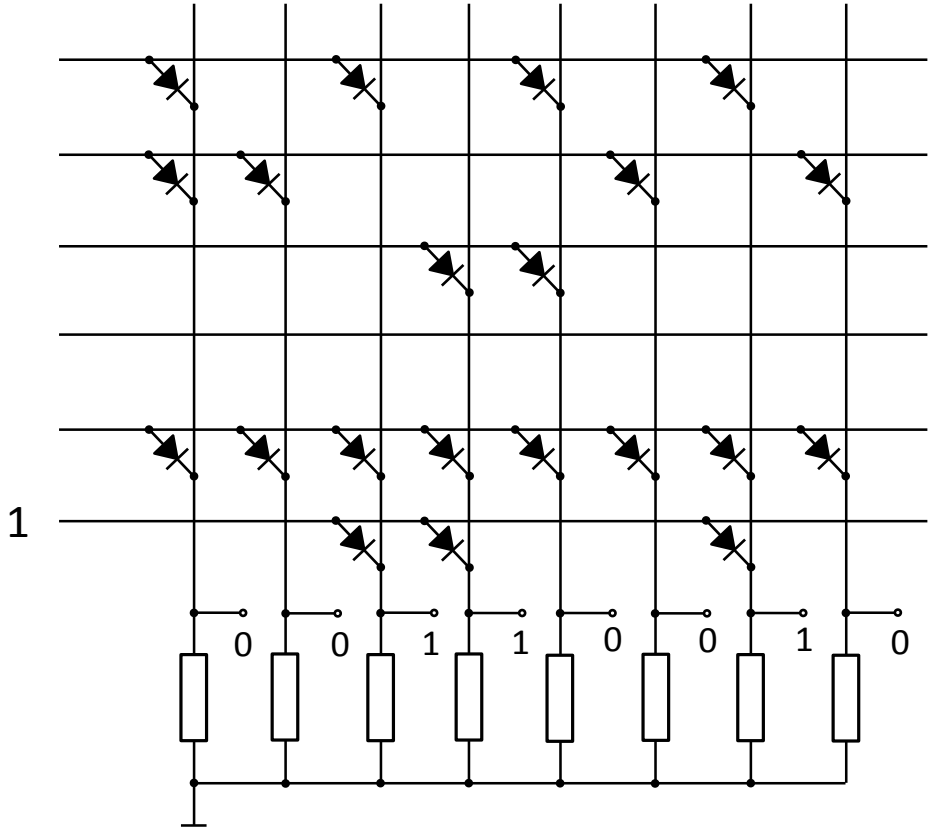
Von der Diode zum Festspeicher

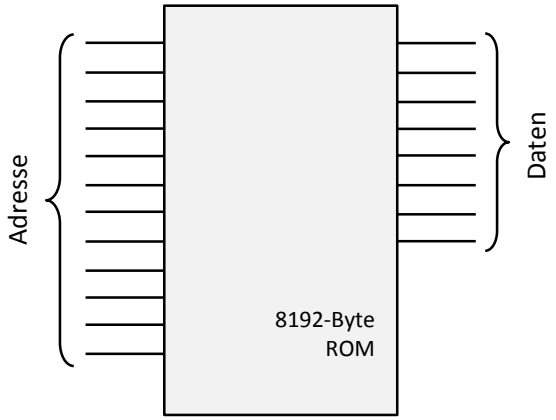




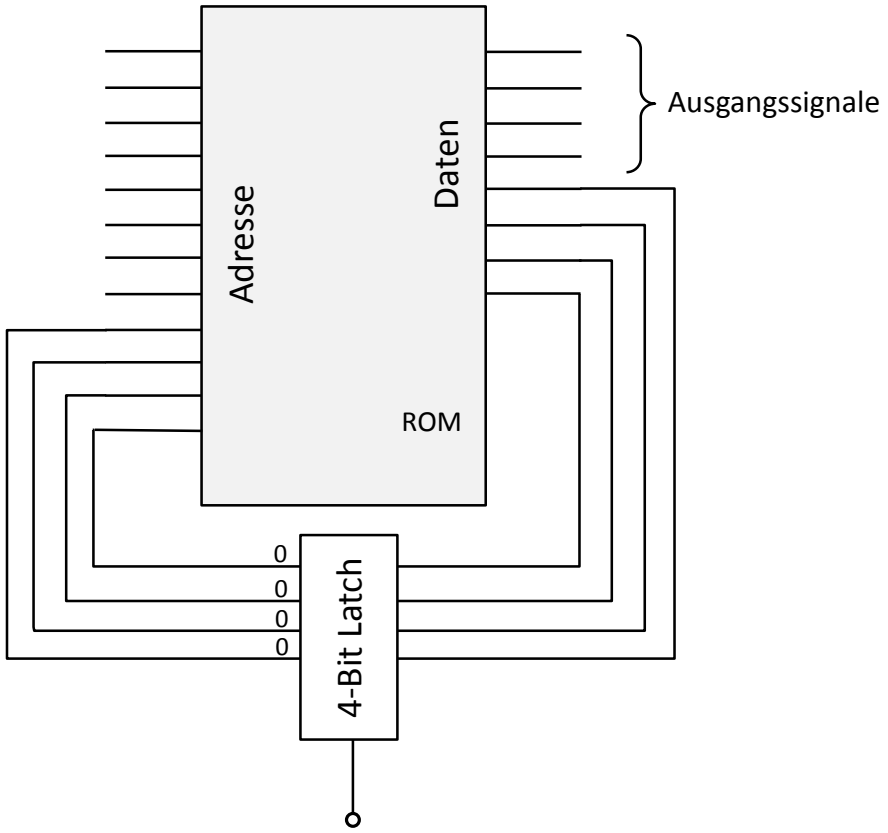
Von der Diode zum Festspeicher



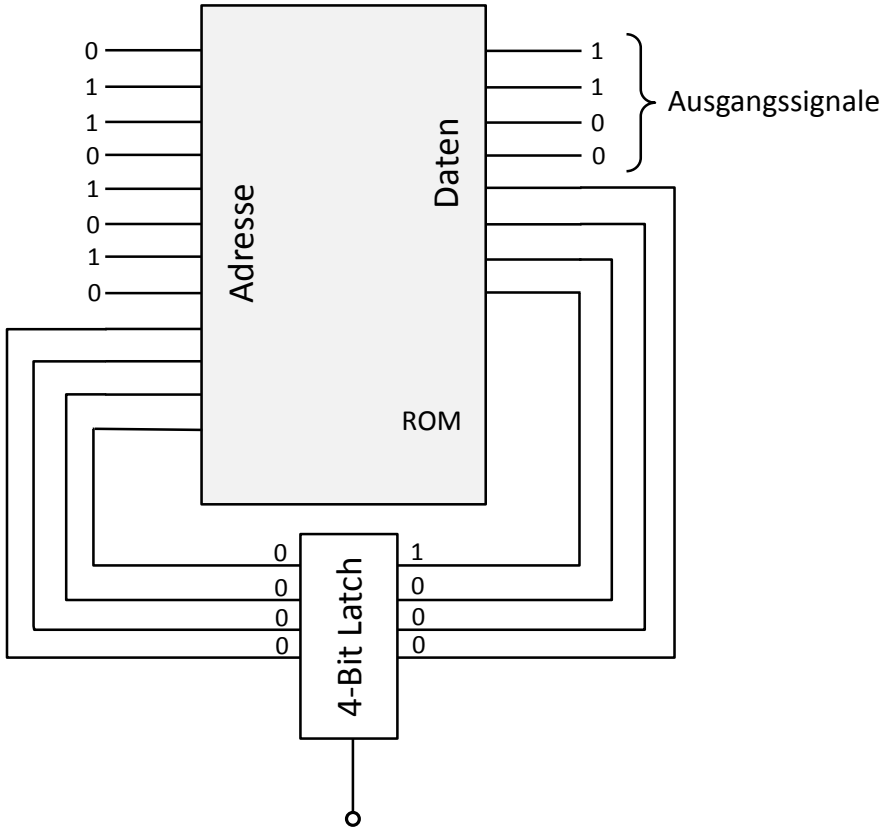




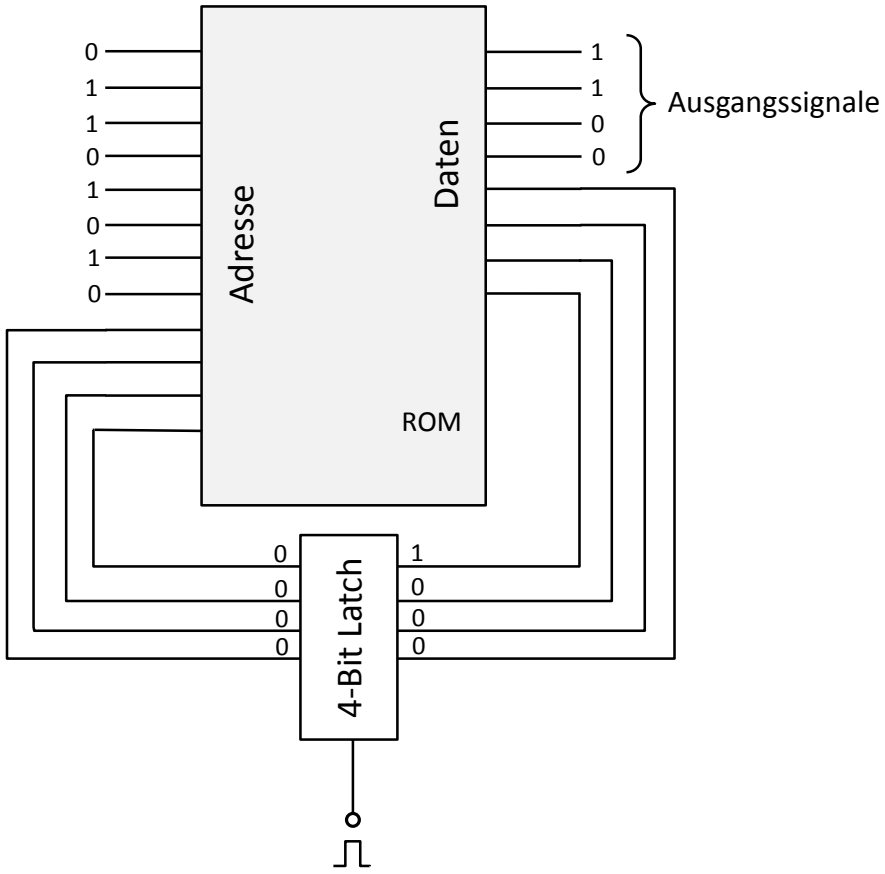
Vom Speicher zur Ablaufsteuerung



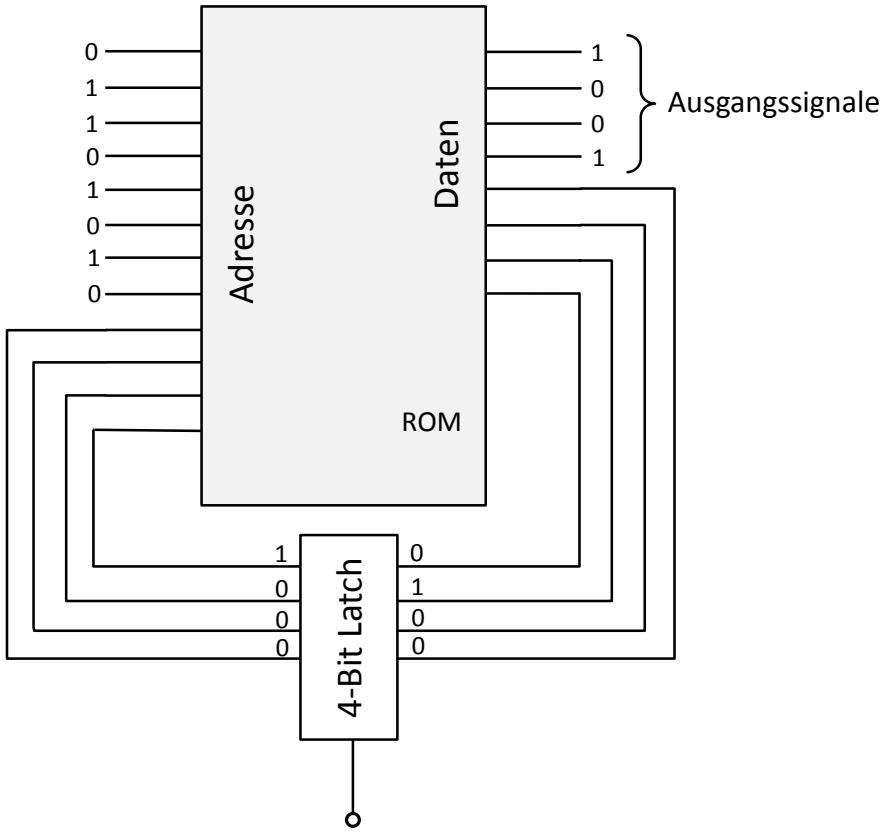
Vom Speicher zur Ablaufsteuerung



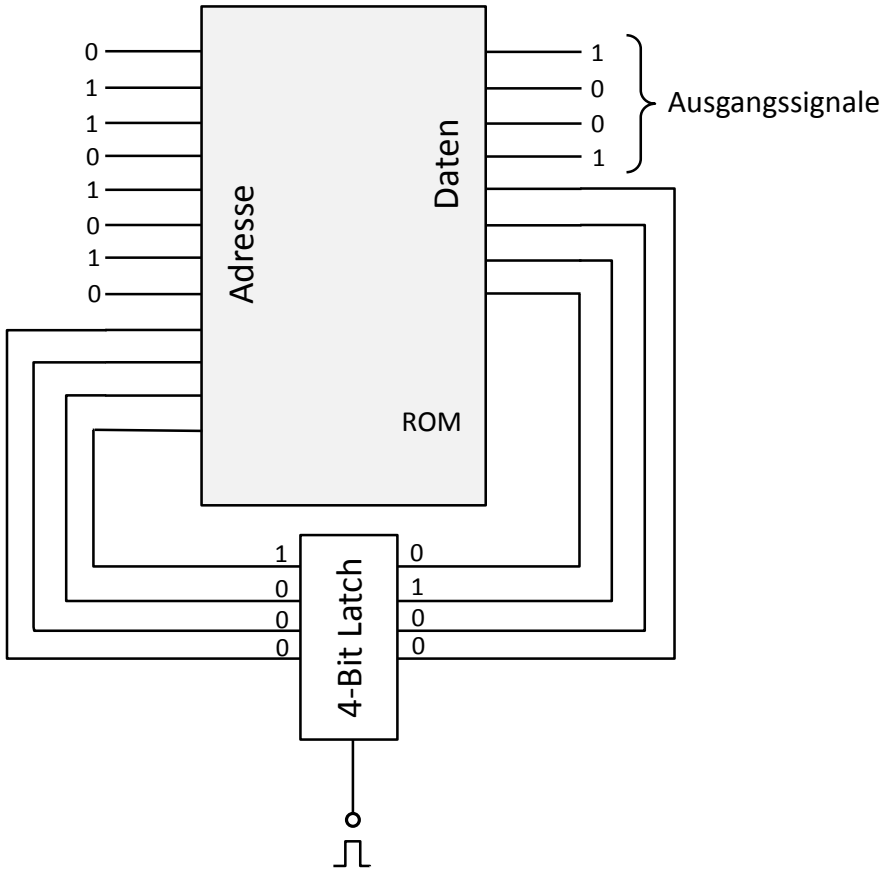
Vom Speicher zur Ablaufsteuerung



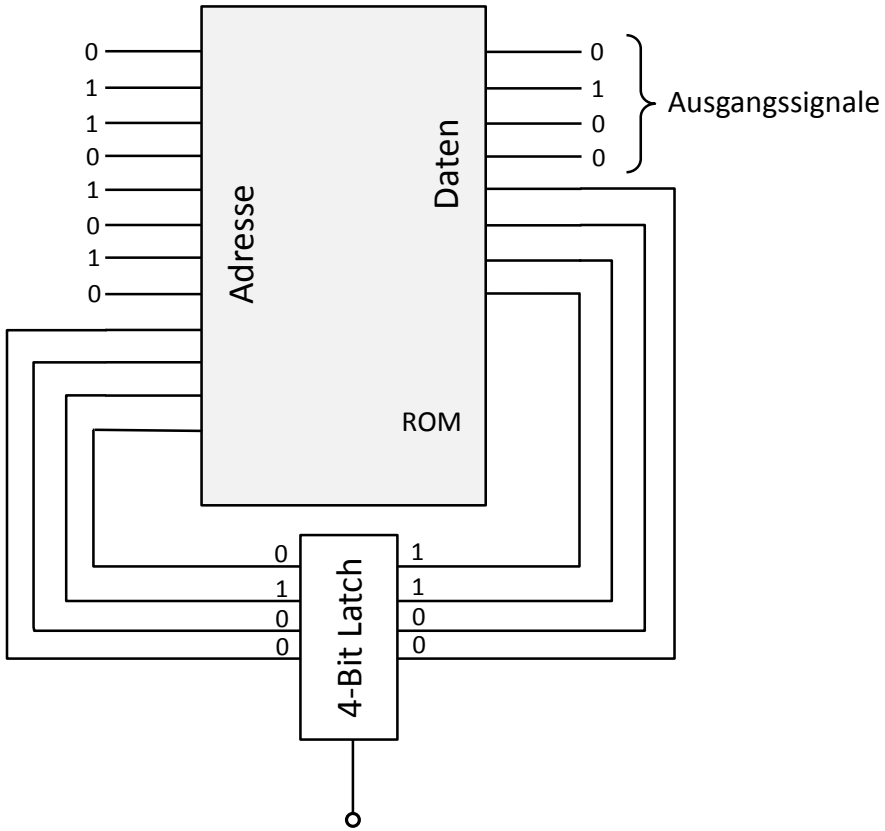
Vom Speicher zur Ablaufsteuerung



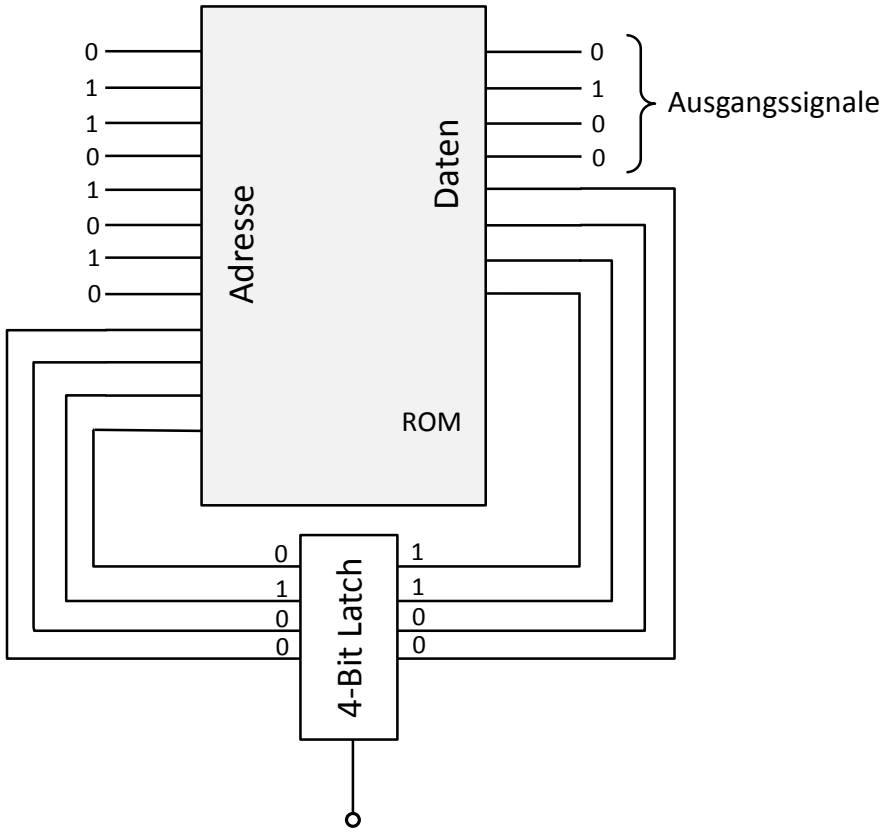
Vom Speicher zur Ablaufsteuerung

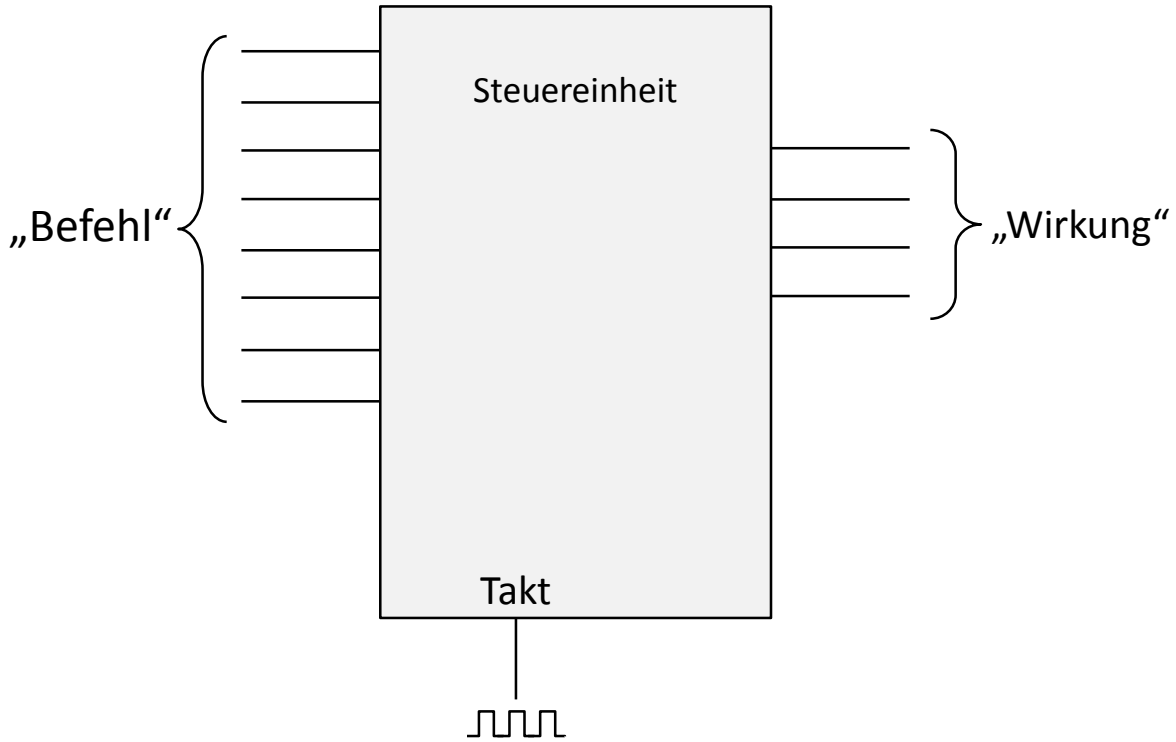


Vom Speicher zur Ablaufsteuerung

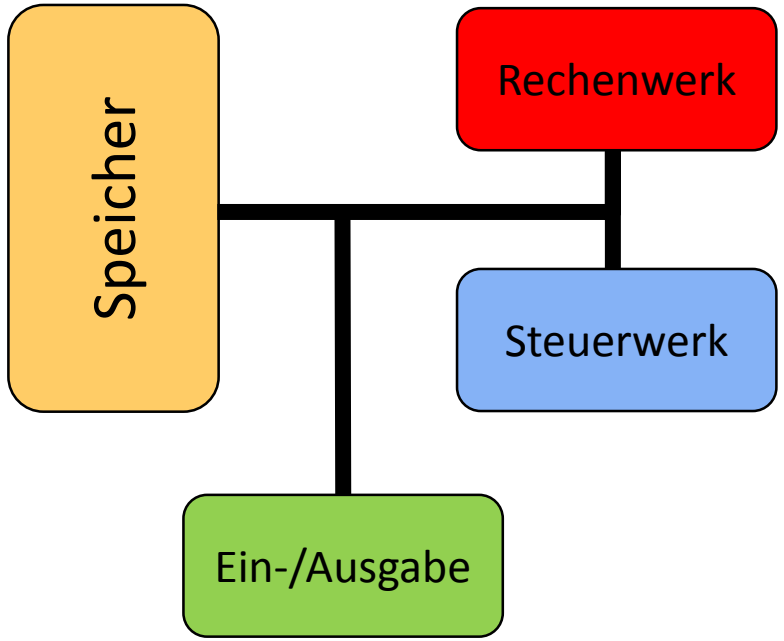


Vom Speicher zur Ablaufsteuerung



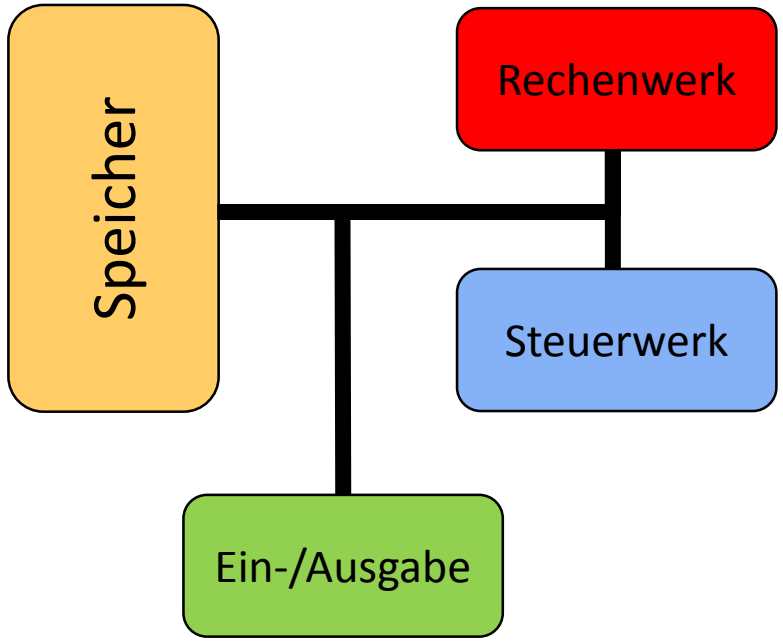


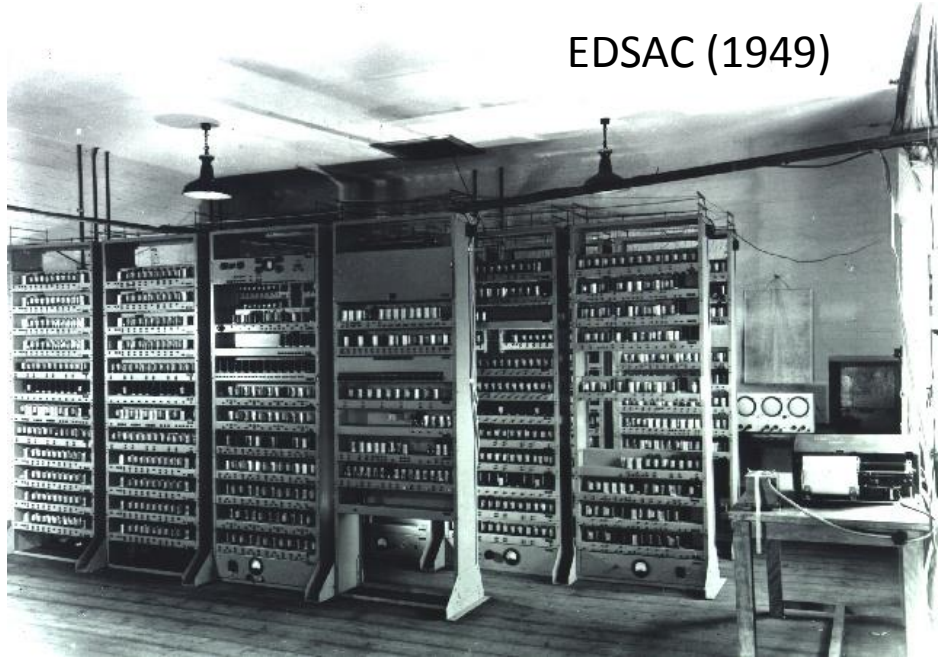
Der von-Neumann-Computer




```
0f 29 5c c7 30      movaps %xmm3,0x30(%rdi,%rax,8)
48 83 c0 08         add    $0x8,%rax
78 a6               js     401b50 <triad_asm+0x4b>
```

Der von-Neumann-Computer

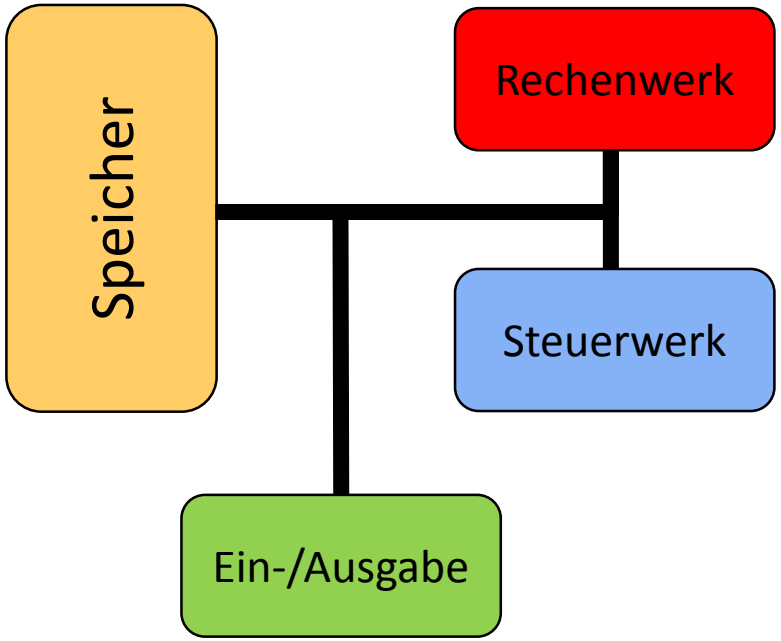




EDSAC (1949)

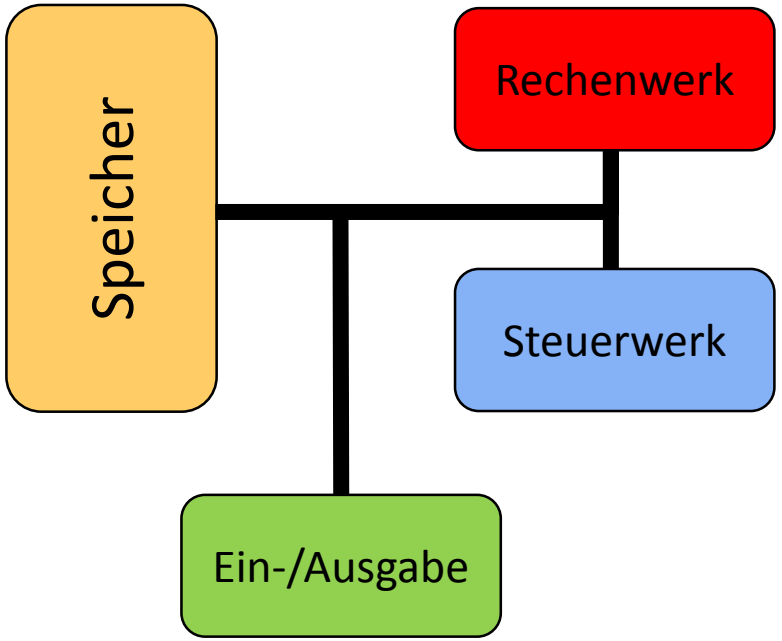

```
0f 29 5c c7 30      movaps %xmm3,0x30(%rdi,%rax,8)
48 83 c0 08         add    $0x8,%rax
78 a6               js     401b50 <triad_asm+0x4b>
```

Der von-Neumann-Computer



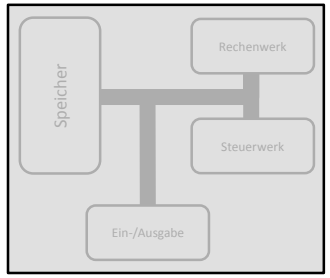

```
0f 29 5c c7 30       movaps %xmm3,0x30(%rdi,%rax,8)
48 83 c0 08          add    $0x8,%rax
78 a6                js     401b50 <triad_asm+0x4b>
```

Der von-Neumann-Computer

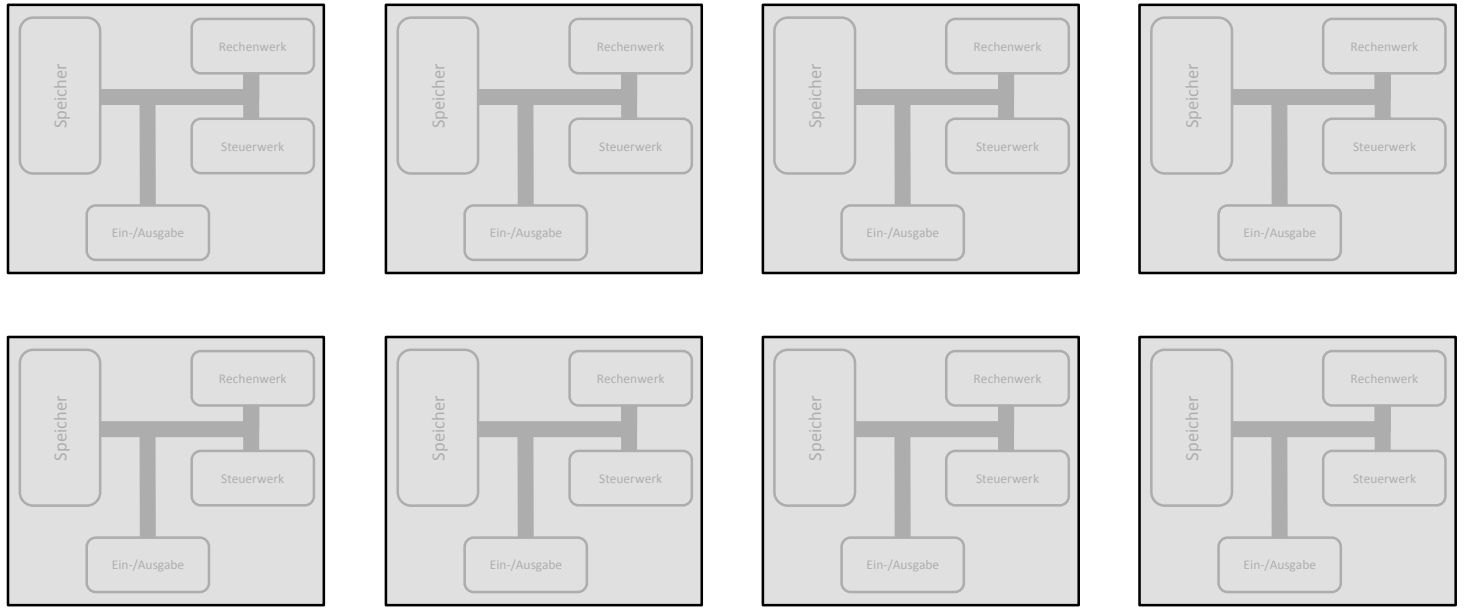



```
0f 29 5c c7 30       movaps %xmm3,0x30(%rdi,%rax,8)
48 83 c0 08          add    $0x8,%rax
78 a6                js     401b50 <triad_asm+0x4b>
```

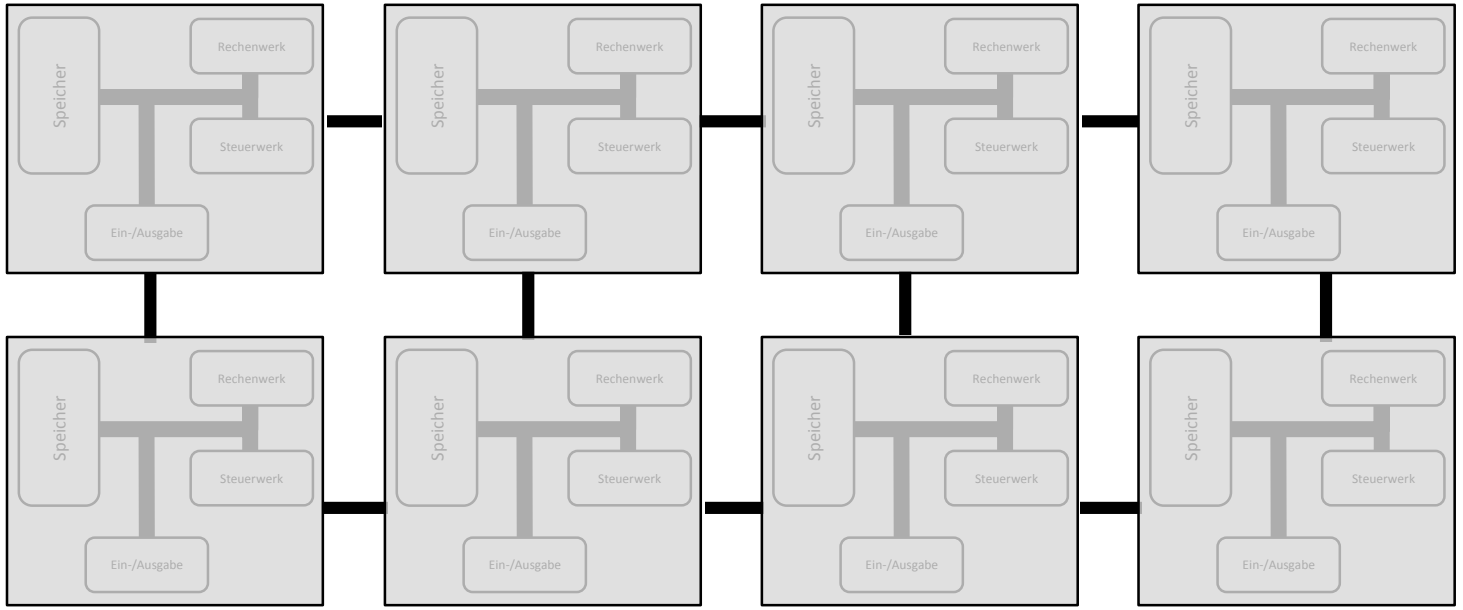
Nicht schnell genug? Parallelisierung!



Nicht schnell genug? Parallelisierung!



Nicht schnell genug? Parallelisierung!



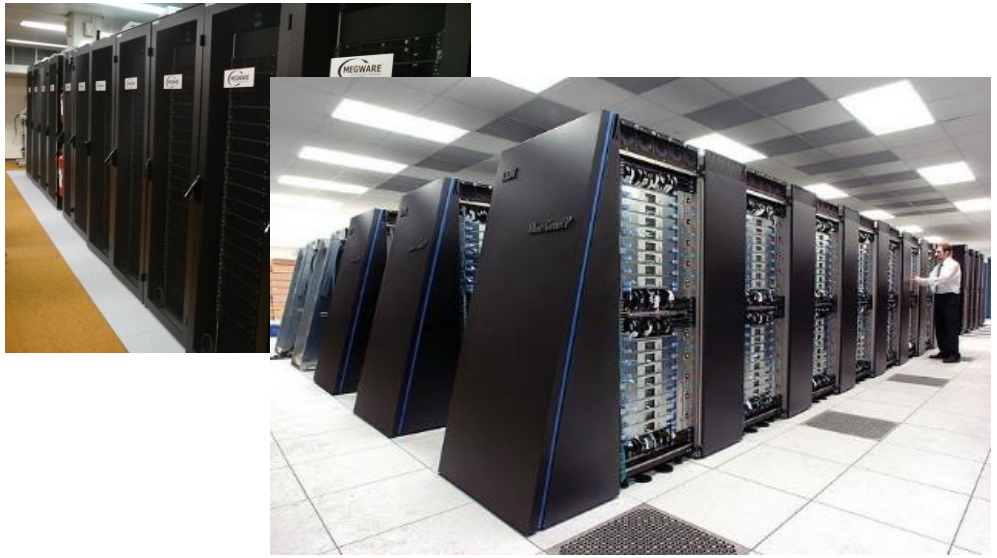
Supercomputer:
Rechnen für Erwachsene

www.top500.org

Supercomputer:
Rechnen für Erwachsene

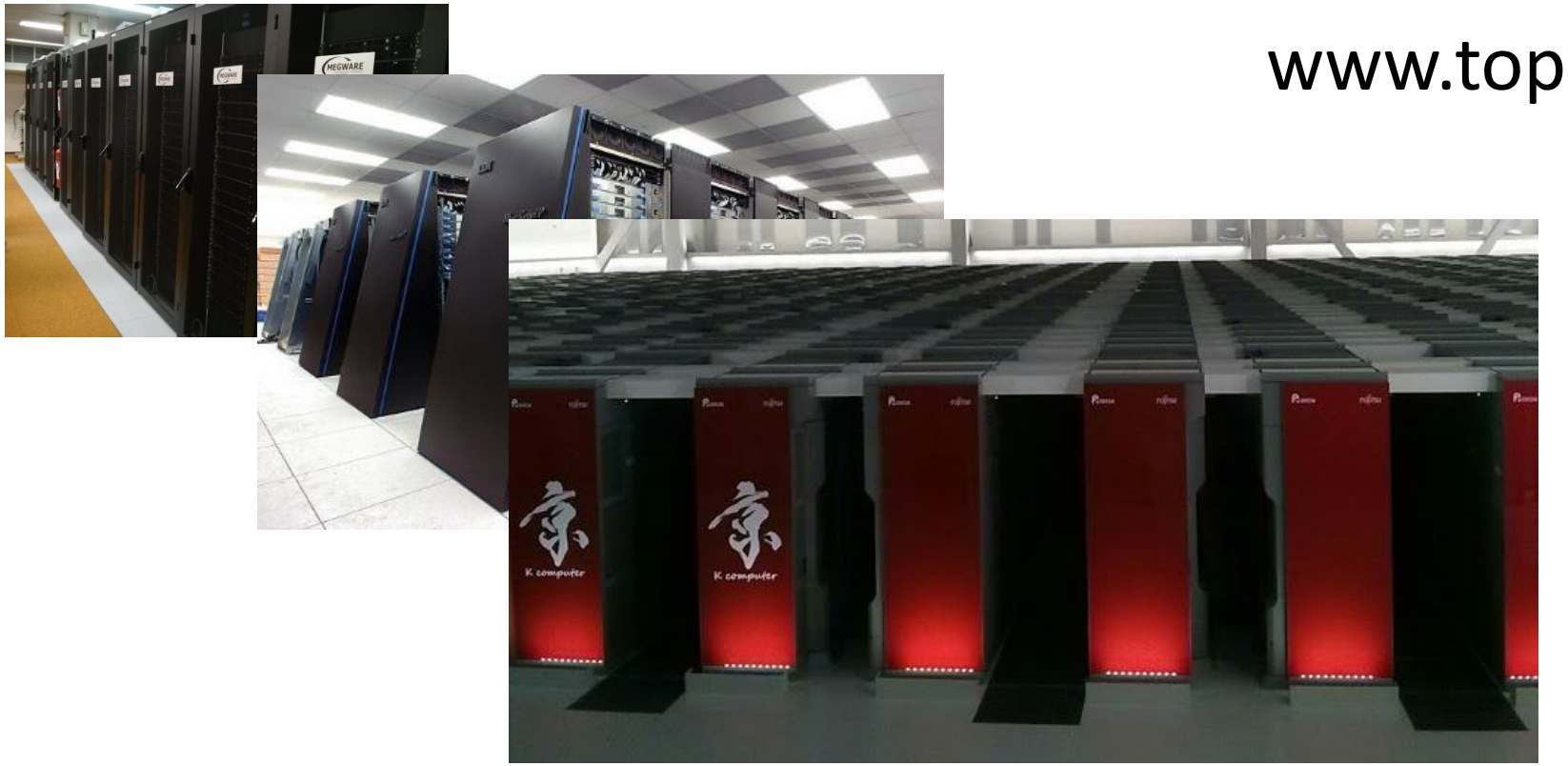
www.top500.org

Supercomputer:
Rechnen für Erwachsene



www.top500.org

Supercomputer:
Rechnen für Erwachsene



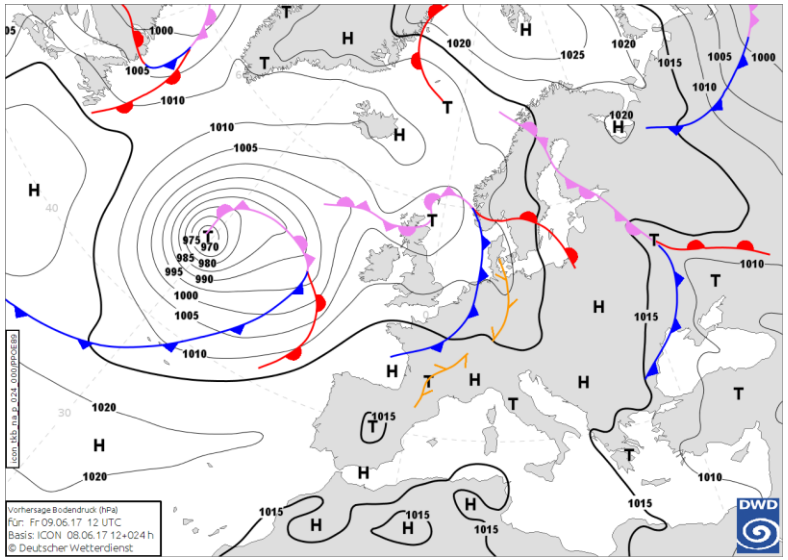
www.top500.org

Supercomputer:
Rechnen für Erwachsene

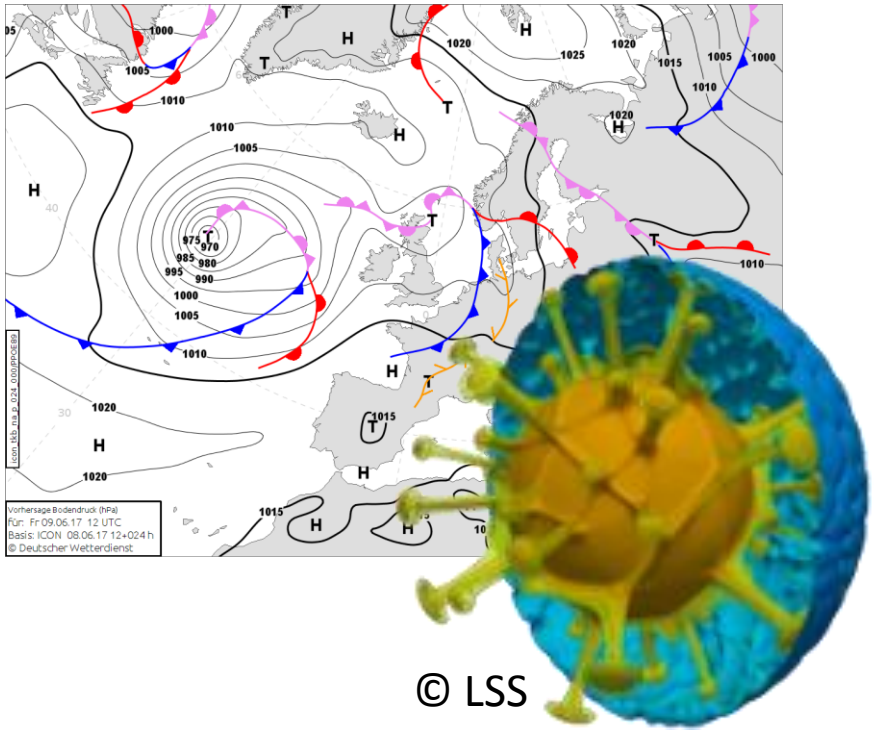
www.top500.org

Aufgaben für Supercomputer

Aufgaben für Supercomputer

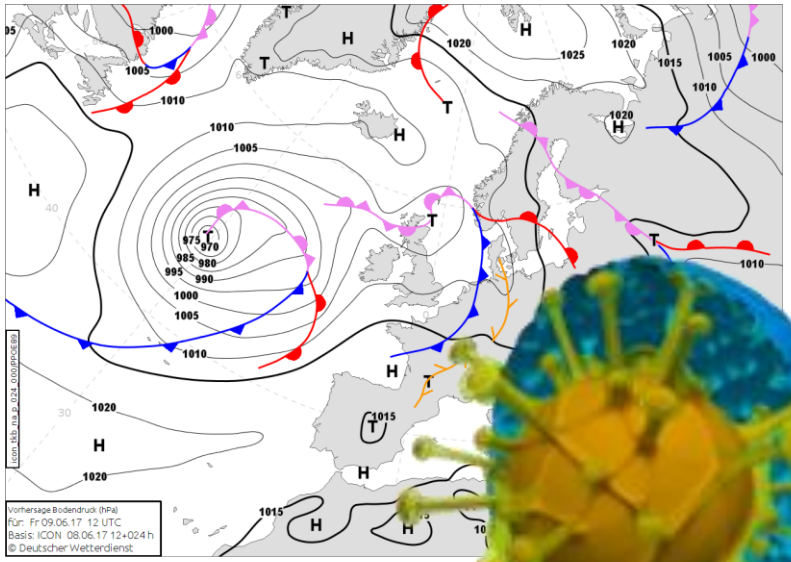


Aufgaben für Supercomputer

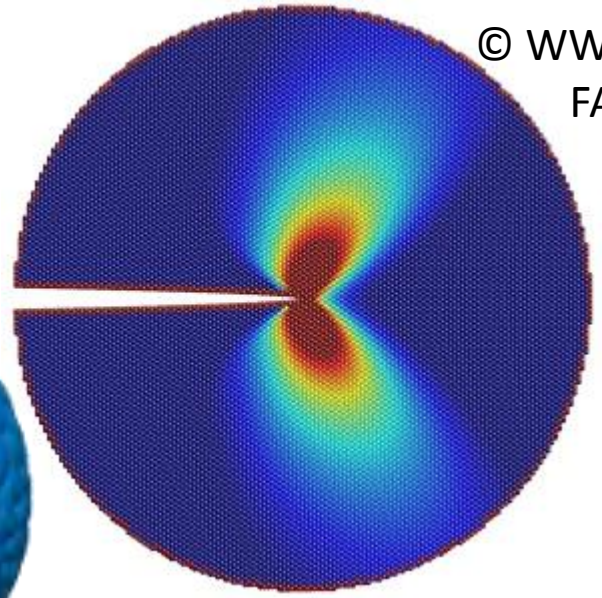


© LSS

Aufgaben für Supercomputer

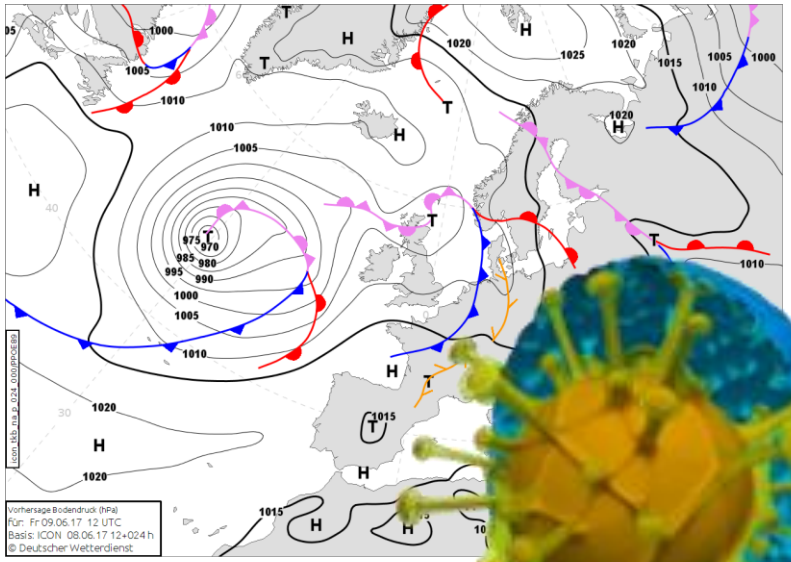


© LSS

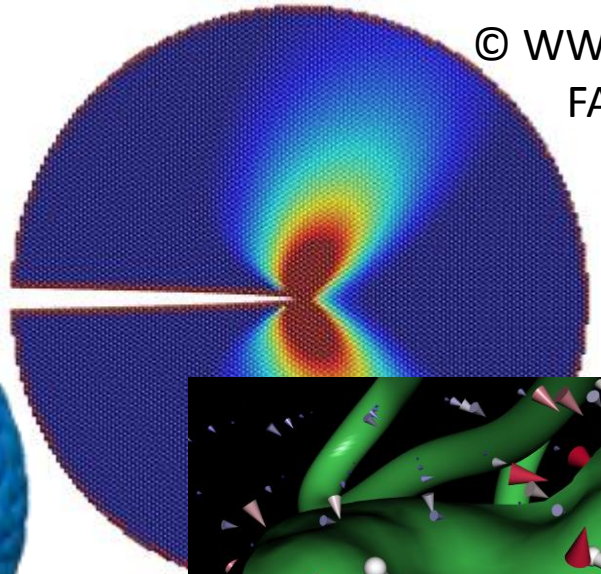


© WW1, FAU

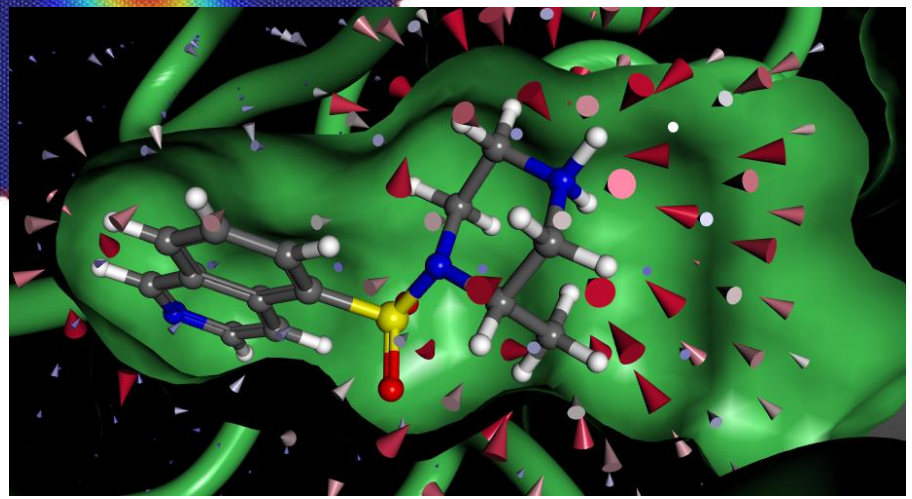
Aufgaben für Supercomputer



© LSS

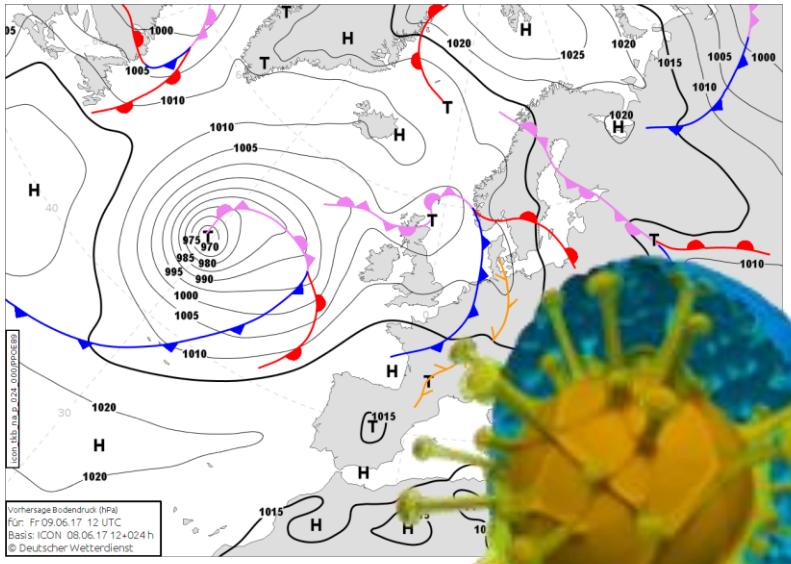


© WW1, FAU

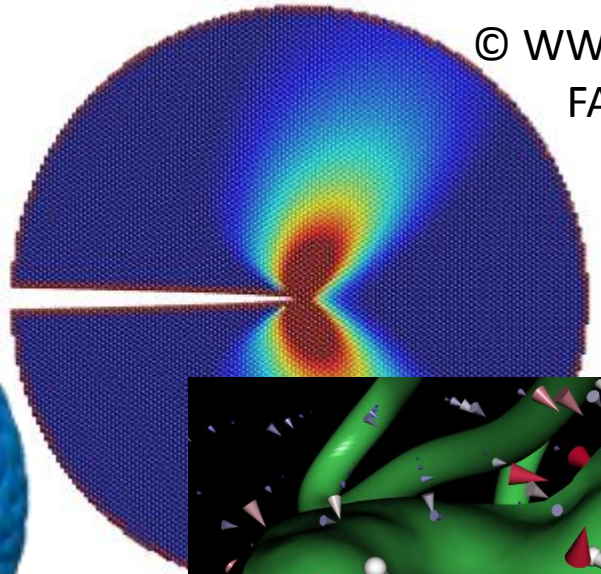


© T. Exner, Molcad GmbH

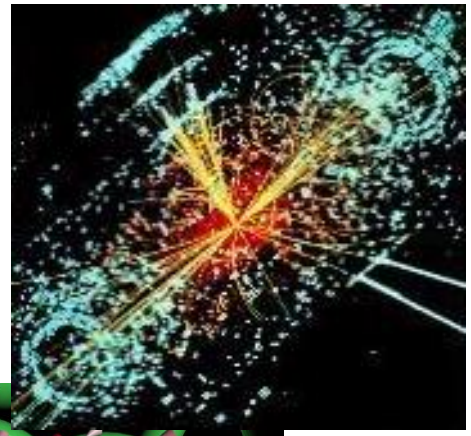
Aufgaben für Supercomputer

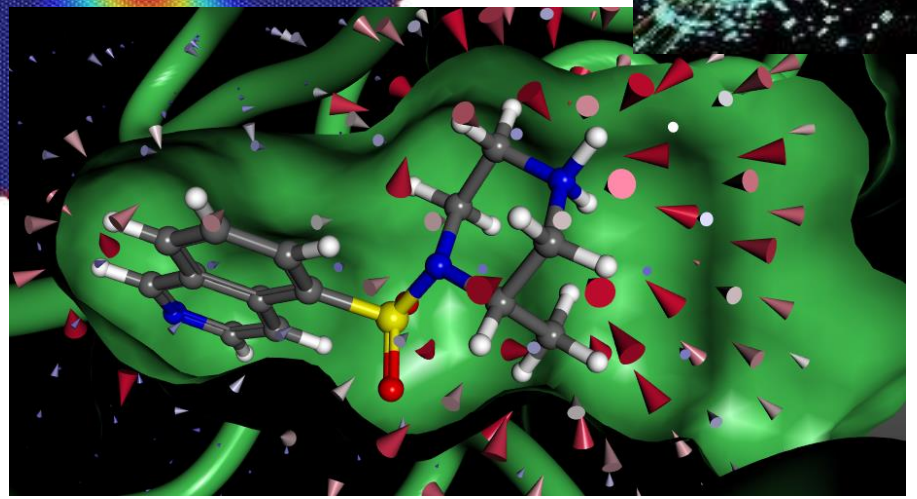


© LSS



© WW1, FAU

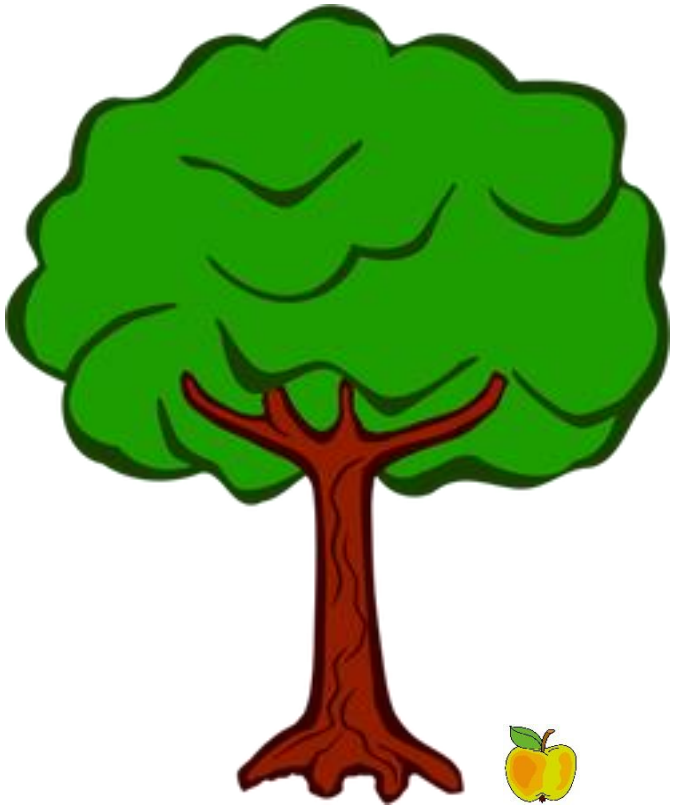




© T. Exner, Molcad GmbH

Von der Physik zum Modell

Von der Physik zum Modell

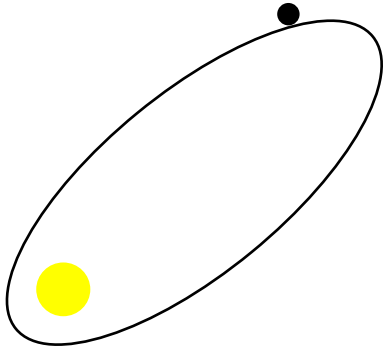


Von der Physik zum Modell

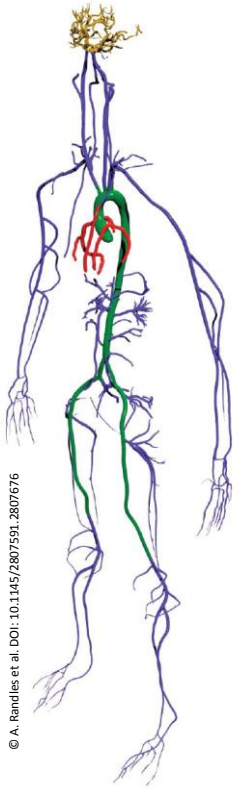
$$\Rightarrow \quad \vec{F} = m \cdot \vec{a}$$

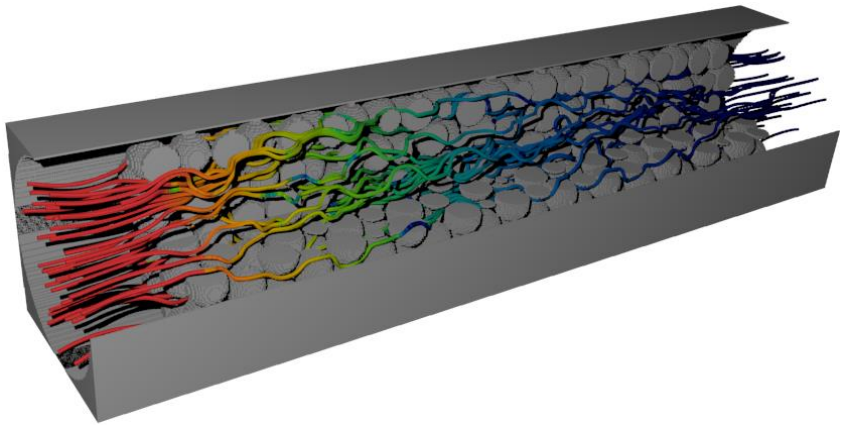
Von der Physik zum Modell

$$\Rightarrow \quad \vec{F} = m \cdot \vec{a} \quad \Rightarrow$$



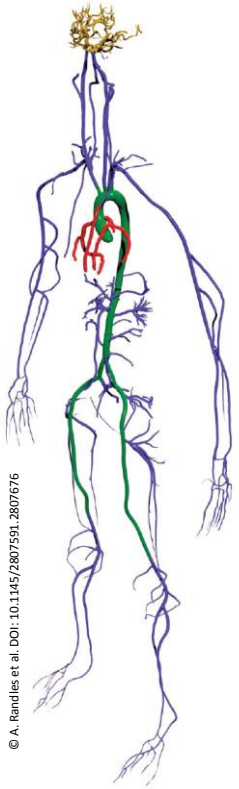
Vom Modell zum Algorithmus

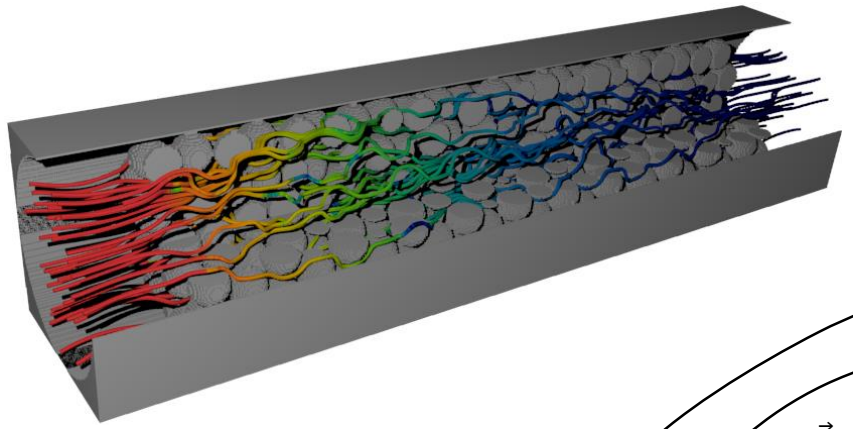


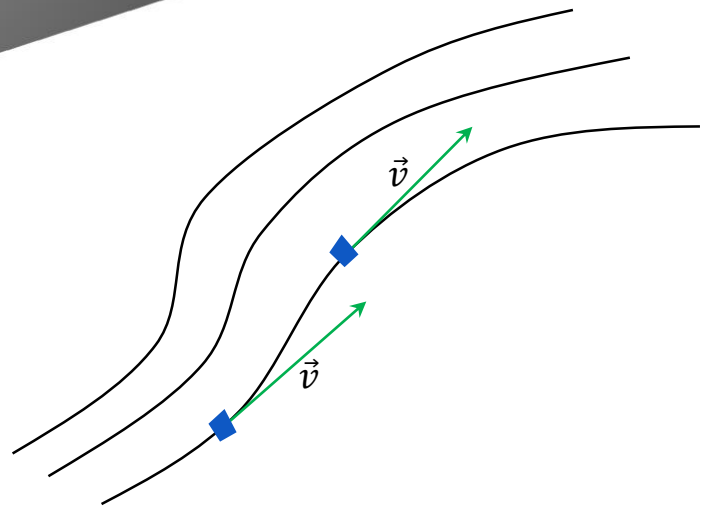


$$\rho\dot{\vec{v}} = \rho\left(\frac{\partial\vec{v}}{\partial t} + (\vec{v}\cdot\nabla)\vec{v}\right) = -\nabla p + \mu\Delta\vec{v} + (\lambda+\mu)\nabla(\nabla\cdot\vec{v}) + \vec{f}.$$

Vom Modell zum Algorithmus

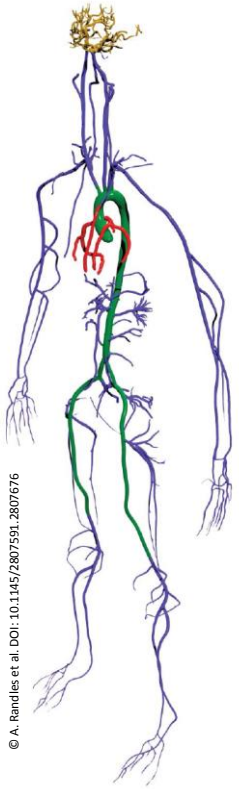


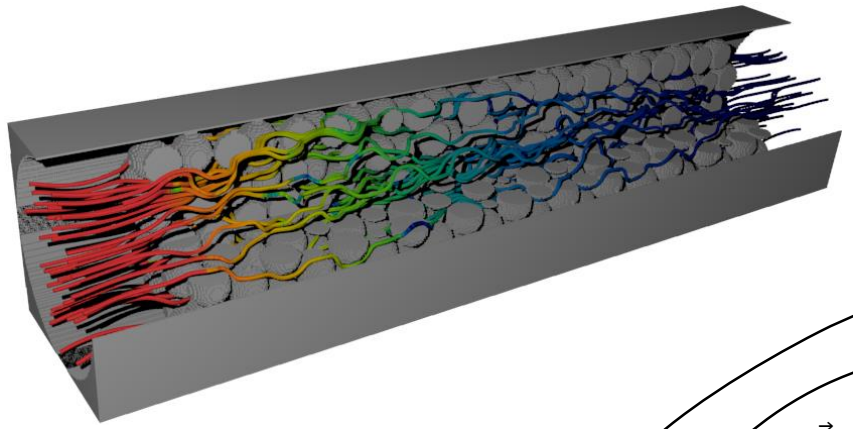


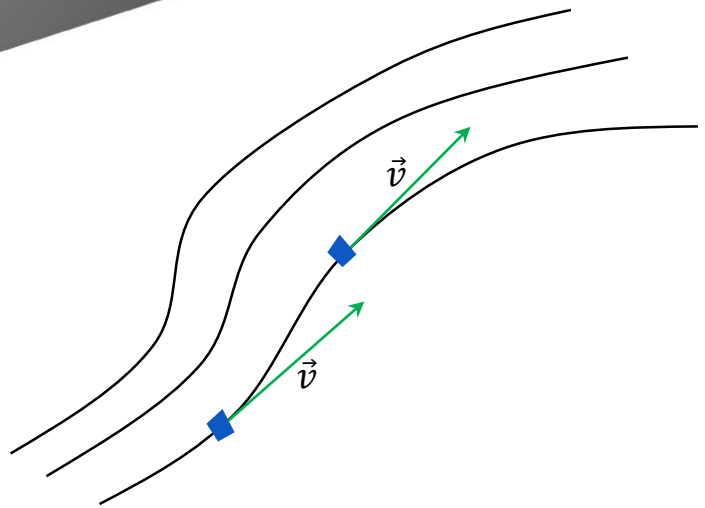


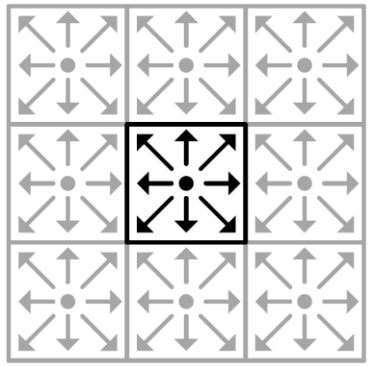
$$\rho\dot{\vec{v}} = \rho\left(\frac{\partial\vec{v}}{\partial t} + (\vec{v}\cdot\nabla)\vec{v}\right) = -\nabla p + \mu\Delta\vec{v} + (\lambda+\mu)\nabla(\nabla\cdot\vec{v}) + \vec{f}.$$

Vom Modell zum Algorithmus



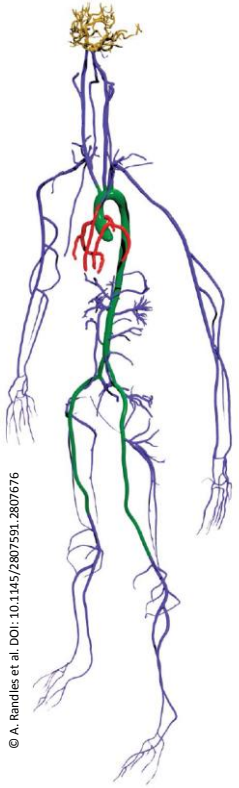


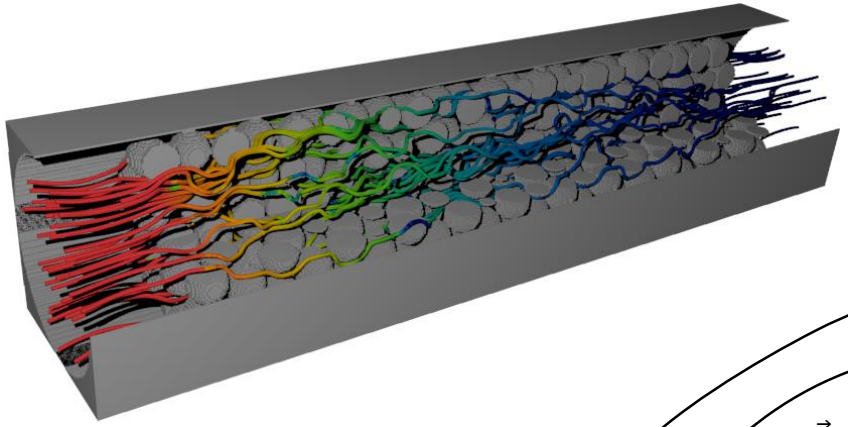


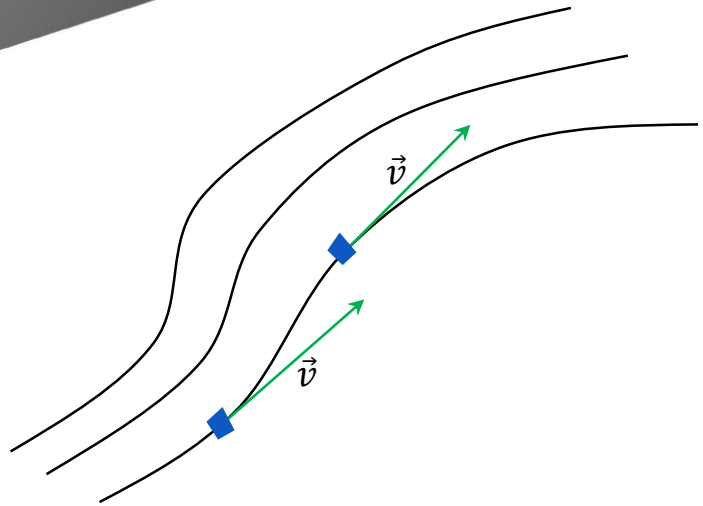


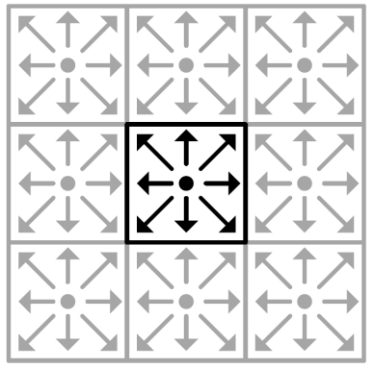
$$\rho\dot{\vec{v}} = \rho\left(\frac{\partial\vec{v}}{\partial t} + (\vec{v}\cdot\nabla)\vec{v}\right) = -\nabla p + \mu\Delta\vec{v} + (\lambda+\mu)\nabla(\nabla\cdot\vec{v}) + \vec{f}.$$

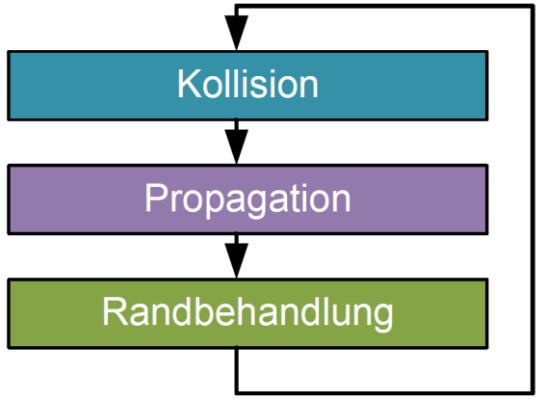
Vom Modell zum Algorithmus





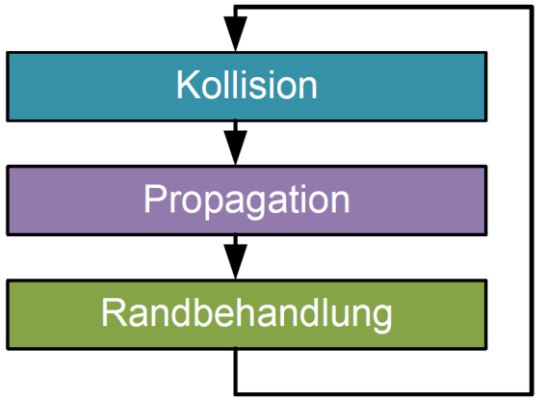




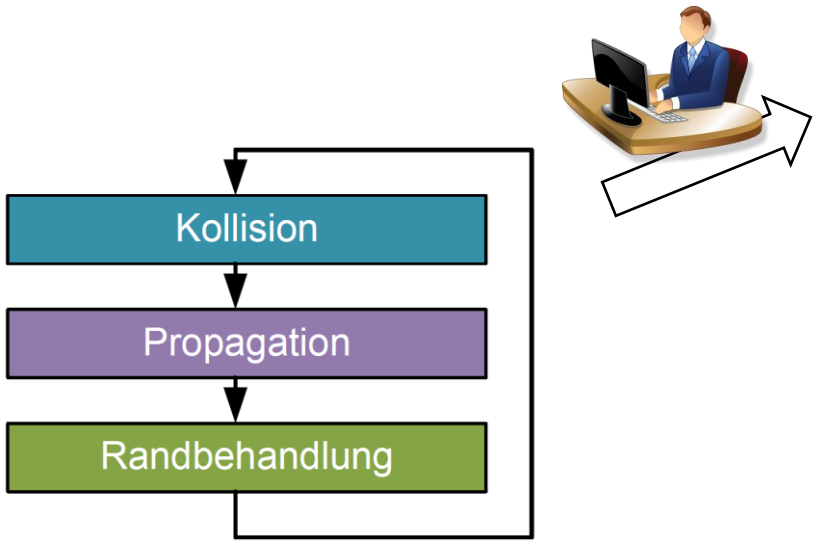


$$\rho\dot{\vec{v}} = \rho\left(\frac{\partial\vec{v}}{\partial t} + (\vec{v}\cdot\nabla)\vec{v}\right) = -\nabla p + \mu\Delta\vec{v} + (\lambda+\mu)\nabla(\nabla\cdot\vec{v}) + \vec{f}.$$

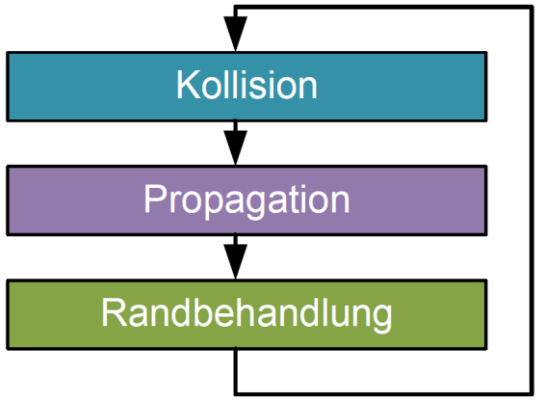
Vom Algorithmus zum Programm



Vom Algorithmus zum Programm

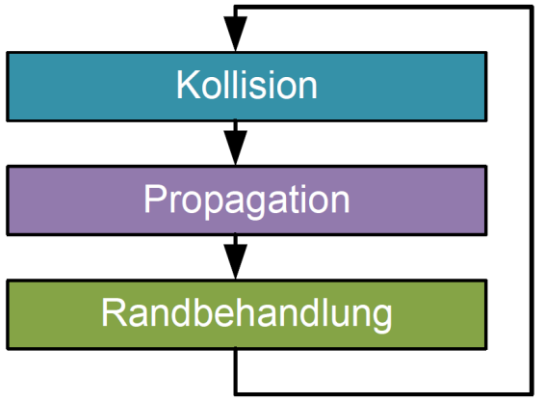


Vom Algorithmus zum Programm

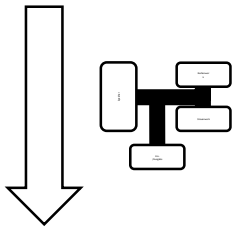


```
      do 260 k = 1,kmax
        do 260 i = 1,imax
          etaref = spec2(i,1,k,mb)
          do 265 j = 1,jmax
            spec2(i,j,k,mb) = spec2(i,j,k,mb) - etaref
265       continue
260   continue
```

Vom Algorithmus zum Programm



```
      do 260 k = 1,kmax
        do 260 i = 1,imax
          etaref = spec2(i,1,k,mb)
          do 265 j = 1,jmax
            spec2(i,j,k,mb) = spec2(i,j,k,mb) - etaref
265       continue
260   continue
```



```
0f 29 5c c7 30      movaps %xmm3,0x30(%rdi,%rax,8)
48 83 c0 08         add    $0x8,%rax
78 a6               js     401b50 <triad_asm+0x4b>
```

Performance (Rechenleistung)

Leistungsmaß:

$$P = \frac{\text{Arbeit}}{\text{Zeit}}$$

Performance (Rechenleistung)

Leistungsmaß:

$$P = \frac{\text{Arbeit}}{\text{Zeit}}$$

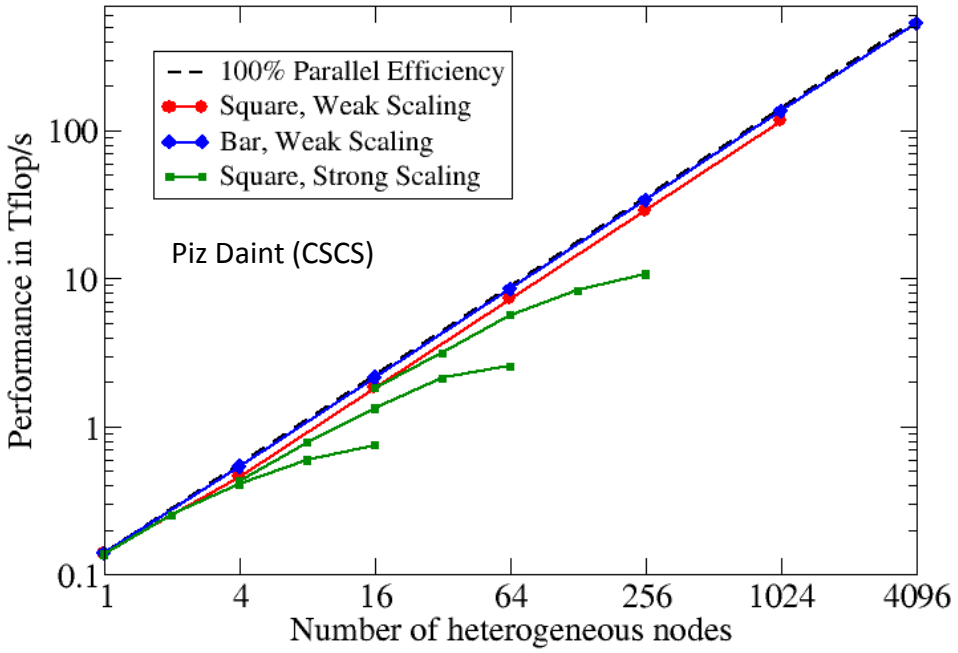
Performance (Rechenleistung)

Leistungsmaß:

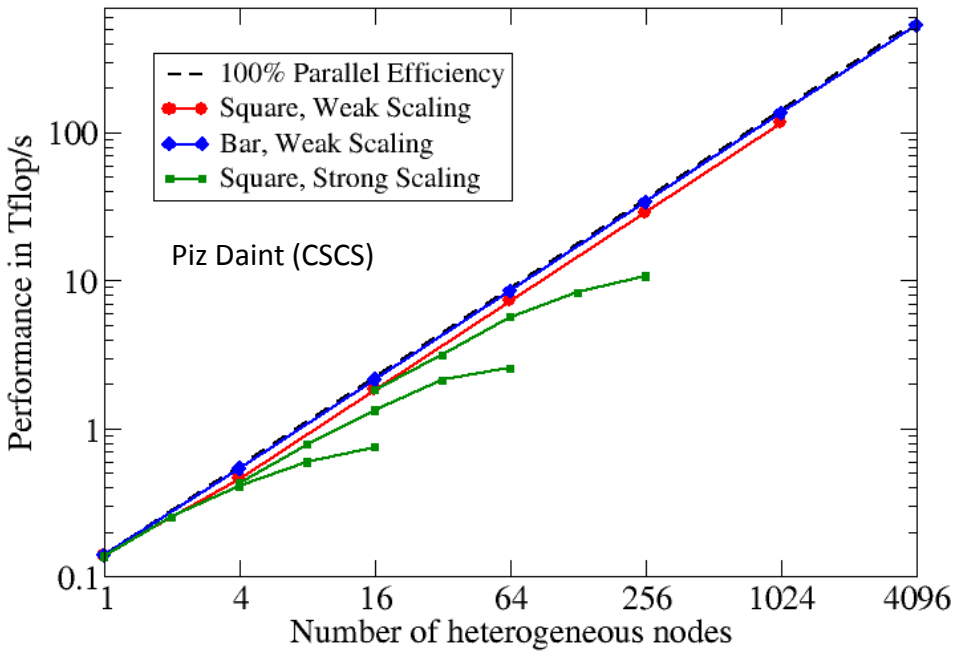
$$P = \frac{\text{Arbeit}}{\text{Zeit}}$$

„Flops“ (+ - * /)
Gitterpunkte
„Durchläufe“
„Lösung des Problems“
…

Performance ist alles! Oder doch nicht?



Performance ist alles! Oder doch nicht?



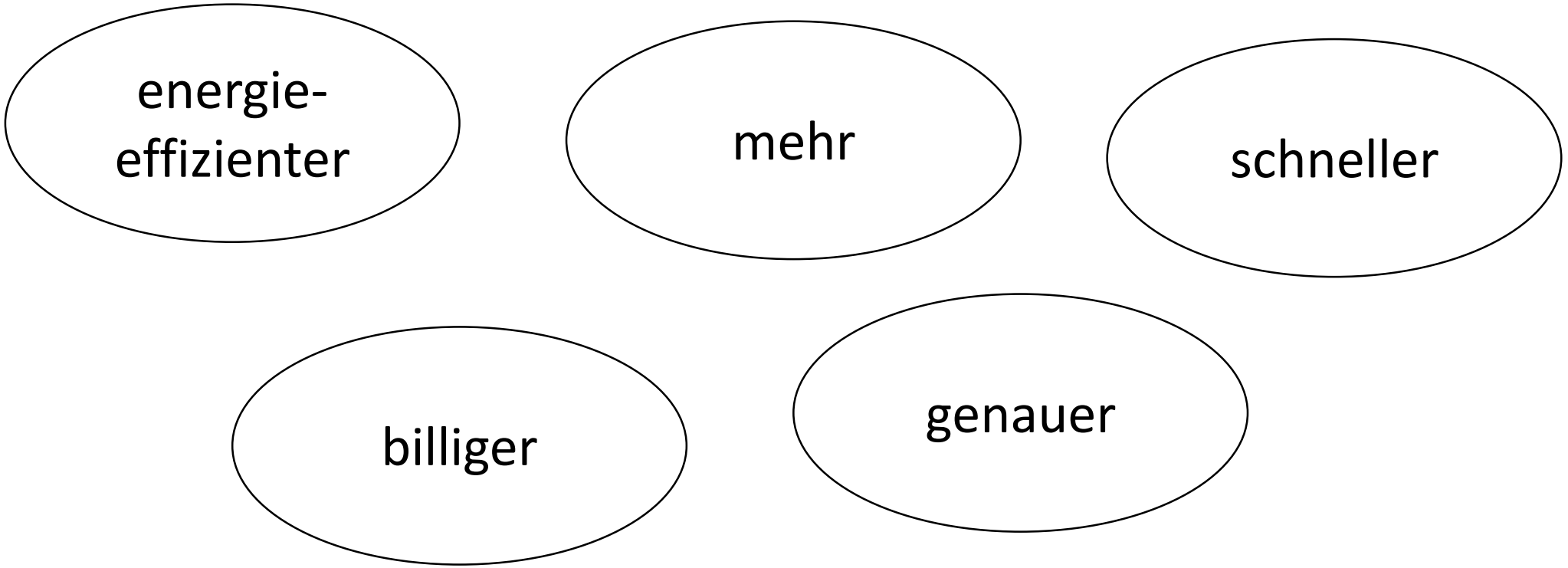
Fragen:

- Ist das das Limit oder geht es noch besser?
- Wie kann ich die teuren Ressourcen möglichst effektiv nutzen?
- Wäre ein anderer Supercomputer besser geeignet?
- Wäre ein anderer Algorithmus noch schneller oder genauer oder beides?

- Wieviel elektrische Energie braucht die Lösung des Problems? Kann man das reduzieren?

Herausforderungen

Herausforderungen



Interessiert? MINT-Student?

ISC-Konferenz 2017

Frankfurt Messe, Mittwoch, 21. Juni 2017

ISC STEM STUDENT DAY & GALA
WEDNESDAY, JUNE 21

WHY A STEM STUDENT DAY?

- To help STEM graduates envision HPC careers
- To introduce avenues for gaining HPC skills
- To present the HPC job landscape for STEM graduates

WHAT'S IN IT FOR STUDENTS?

- Insight into a new field & great careers
- Get together with 199 other regional & international STEM students
- Fun day of great food & conversations

Day Program at Messe Frankfurt, Halle 3

3:00 pm – 4:00 pm	**Guided Tour of the ISC 2017 Exhibition**
4:00 pm – 4:15 pm	**Tour of the Student Cluster Competition**
4:15 pm – 5:15 pm	**Explore the Exhibition on Your Own**
5:15 pm – 5:30 pm	**Watch the Student Cluster Competition Awarding**
5:30 pm – 6:15 pm	**Attend HPC Expert Thomas Sterling's Keynote**

Evening Program at Marriott Frankfurt

7:00 pm - 7:15 pm	**Welcome and Drinks**
7:10 pm - 7:20 pm	**Welcome Address by the Event's Main Sponsor**
7:20 pm - 8:00 pm	**Keynote Address by HPC Industry Expert Steve Conway and Prof. Dr. Michael Bader (TUM)**
8:00 pm - 9:30 pm	**Career Fair, Dinner & Networking**

If you are interested in attending the ISC STEM Student Day for free, please visit:

www.isc-hpc.com/stem-student-day-gala.html

ISC High Performance "The HPC Event."