Roofline: A Throughput Oriented Performance Model

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Why Use Performance Models or Tools?

- Identify performance bottlenecks
- Motivate software optimizations
- **Determine when we're done optimizing**
  - Assess performance relative to machine capabilities
  - Motivate need for algorithmic changes
- Predict performance on future machines / architectures
  - Sets realistic expectations on performance for future procurements
  - Used for HW/SW Co-Design to ensure future architectures are well-suited for the computational needs of today's applications.

Performance Models

- Many different components can contribute to kernel run time.
- Some are characteristics of the application, some are characteristics of the machine, and some are both (memory access pattern + caches).

#FP operations	Flop/s
Cache data movement	Cache GB/s
DRAM data movement	DRAM GB/s
PCIe data movement	PCIe bandwidth
Depth	OMP Overhead
MPI Message Size	Network Bandwidth
MPI Send:Wait ratio	Network Gap
#MPI Wait’s	Network Latency

Performance Models

- Can’t think about all these terms all the time for every application…

Computational Complexity

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Performance Models

- Because there are so many components, performance models often conceptualize the system as being dominated by one or more of these components.

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Roofline Model

Williams et al, "Roofline: An Insightful Visual Performance Model For Multicore Architectures", CACM, 2009.

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LogCA

Bin Altaf et al, "LogCA: A High-Level Performance Model for Hardware Accelerators", ISCA, 2017.

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LogGP

Alexandrov, et al, "LogGP: incorporating long messages into the LogP model - one step closer towards a realistic model for parallel computation", SPAA, 1995.

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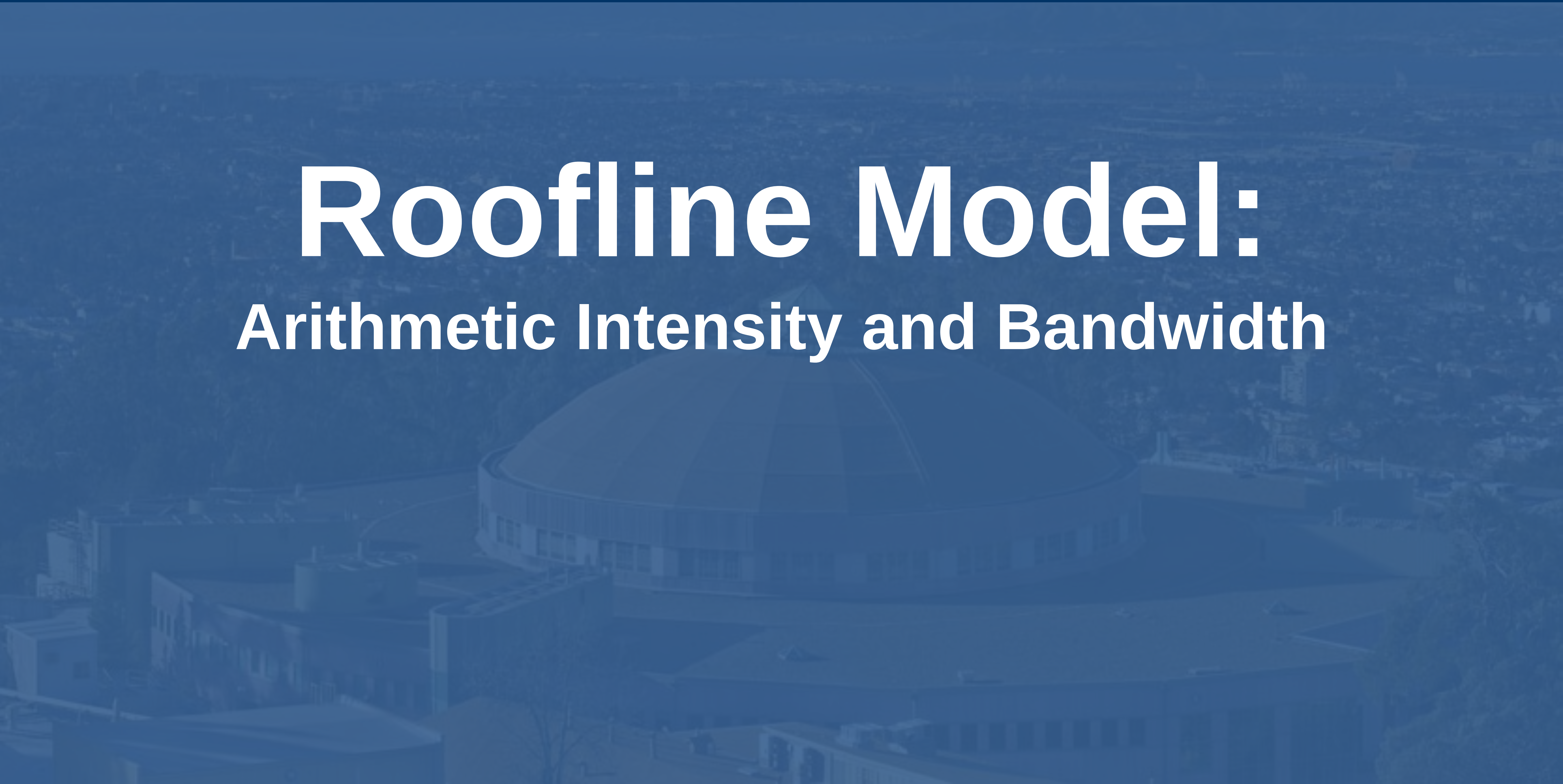
LogP

Right model depends on app and problem size

Culler, et al, "LogP: a practical model of parallel computation", CACM, 1996.



Roofline Model:

Arithmetic Intensity and Bandwidth

Performance Models / Simulators

- Historically, many performance models and simulators tracked latencies to predict performance (i.e. counting cycles)

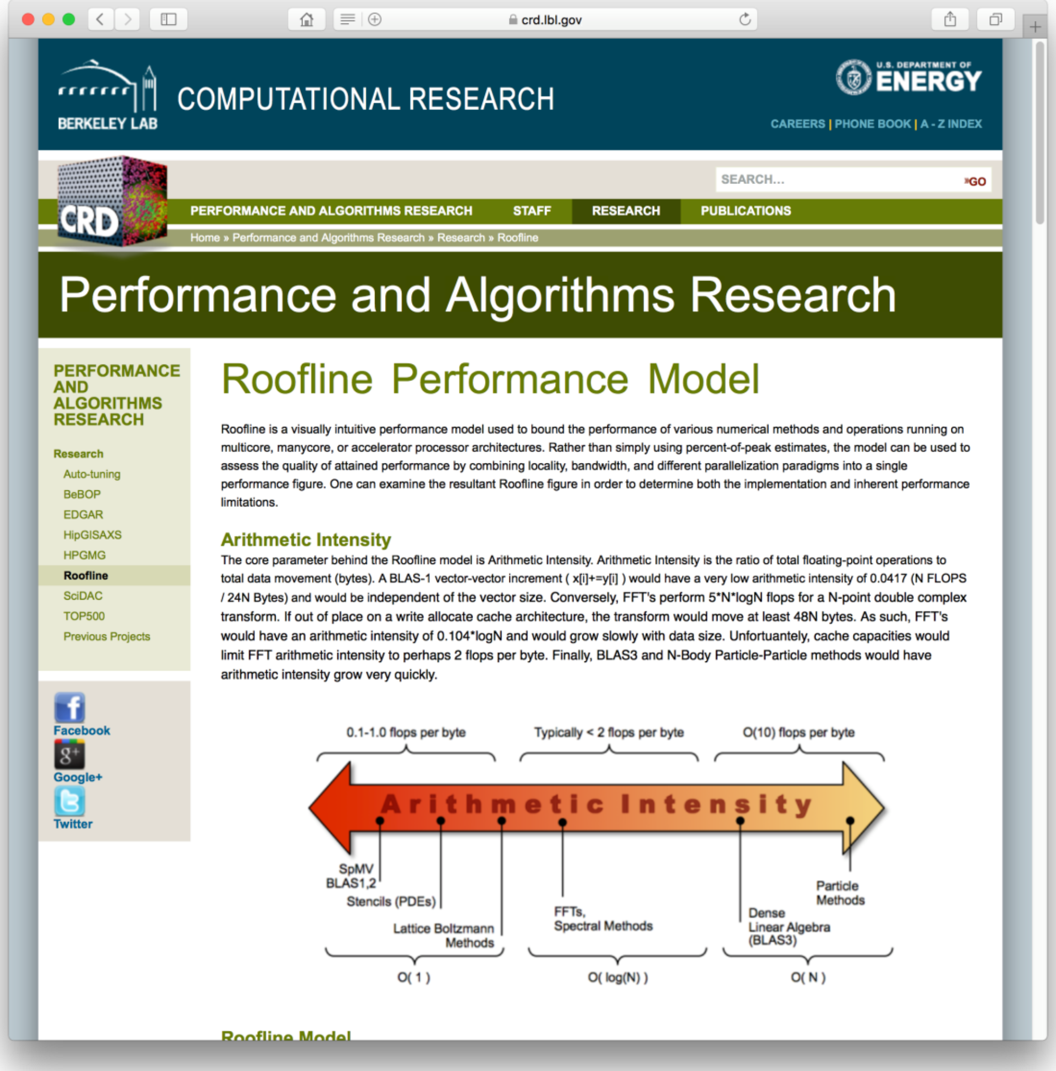
- The last two decades saw a number of latency-hiding techniques…
  - Out-of-order execution (hardware discovers parallelism to hide latency)
  - HW stream prefetching (hardware speculatively loads data)
  - Massive thread parallelism (independent threads satisfy the latency-bandwidth product)

- Effective latency hiding has resulted in a shift from a latency-limited computing regime to a **throughput-limited computing regime**

Roofline Model

- **Roofline Model** is a throughput-oriented performance model…
  - Tracks rates not times
  - Augmented with Little's Law

    (concurrency = latency*bandwidth)
  - Independent of ISA and architecture (applies to CPUs, GPUs, Google TPUs[1], etc…)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Performance and Algorithms Research

Roofline Performance Model

Roofline is a visually intuitive performance model used to bound the performance of various numerical methods and operations running on multicore, manycore, or accelerator processor architectures. Rather than simply using percent-of-peak estimates, the model can be used to assess the quality of attained performance by combining locality, bandwidth, and different parallelization paradigms into a single performance figure. One can examine the resultant Roofline figure in order to determine both the implementation and inherent performance limitations.

Arithmetic Intensity

The core parameter behind the Roofline model is Arithmetic Intensity. Arithmetic Intensity is the ratio of total floating-point operations to total data movement (bytes). A BLAS-1 vector-vector increment (x[i]+=y[i]) would have a very low arithmetic intensity of 0.0417 (N FLOPS / 24N Bytes) and would be independent of the vector size. Conversely, FFT's perform 5*N*logN flops for a N-point double complex transform. If out of place on a write allocate cache architecture, the transform would move at least 48N bytes. As such, FFT's would have an arithmetic intensity of 0.104*logN and would grow slowly with data size. Unfortuantely, cache capacities would limit FFT arithmetic intensity to perhaps 2 flops per byte. Finally, BLAS3 and N-Body Particle-Particle methods would have arithmetic intensity grow very quickly.

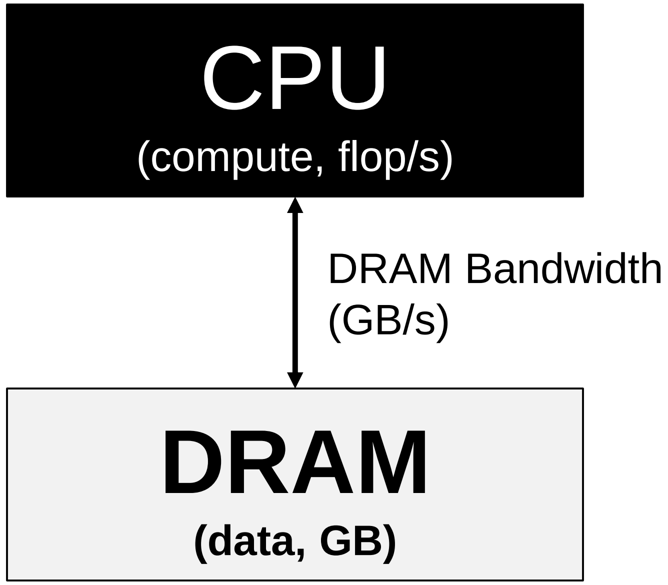
Roofline Model

https://crd.lbl.gov/departments/computer-science/PAR/research/roofline

[1] Jouppi et al, "In-Datacenter Performance Analysis of a Tensor Processing Unit", ISCA, 2017.

(DRAM) Roofline

- One could hope to always attain peak performance (Flop/s)
- However, finite locality (reuse) and bandwidth limit performance.
- Assume:
  - Idealized processor/caches
  - Cold start (data in DRAM)



CPU
(compute, flop/s)

DRAM Bandwidth
(GB/s)

DRAM
(data, GB)

$$\textbf{Time} = \max\begin{cases}\#\textbf{FP ops / Peak GFlop/s}\\ \#\textbf{Bytes / Peak GB/s}\end{cases}$$

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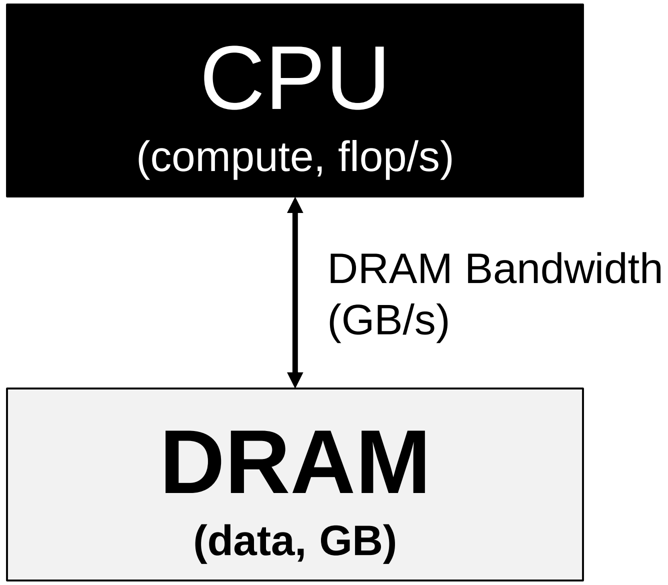

$$\frac{\text{Time}}{\text{\#FP ops}} = \max \begin{cases} 1 / \text{Peak GFlop/s} \\ \text{\#Bytes / \#FP ops / Peak GB/s} \end{cases}$$

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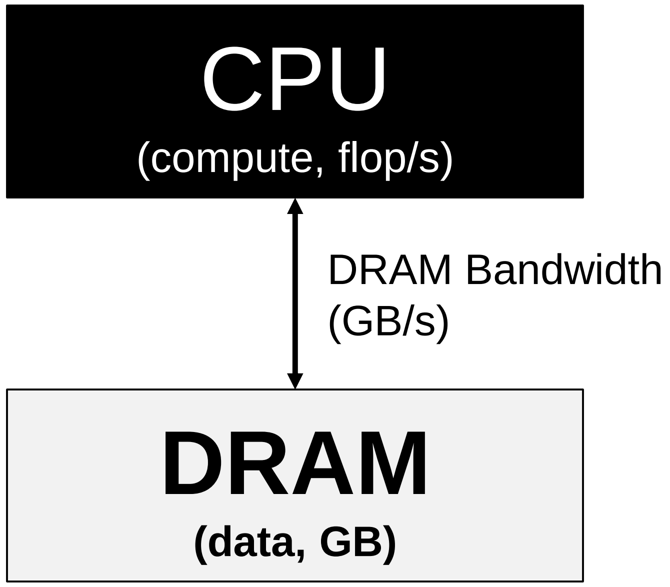

CPU

(compute, flop/s)

DRAM Bandwidth
(GB/s)

DRAM

(data, GB)

$$\frac{\text{\#FP ops}}{\text{Time}} = \min\begin{cases} \text{Peak GFlop/s} \\ \text{(\#FP ops / \#Bytes) * Peak GB/s} \end{cases}$$

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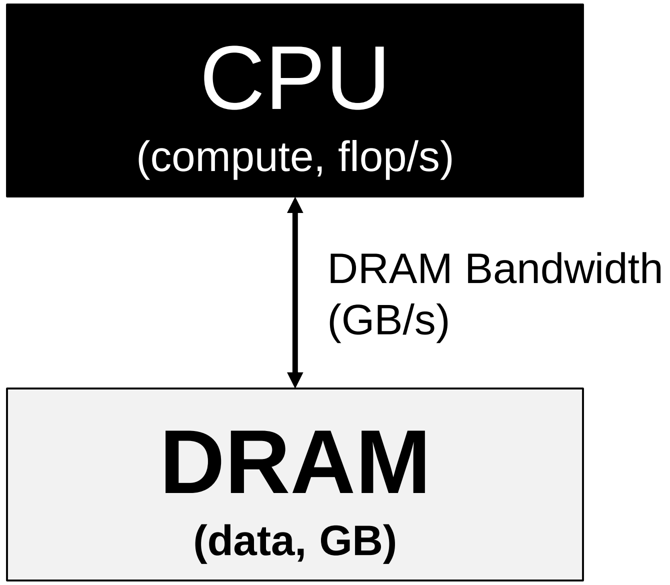
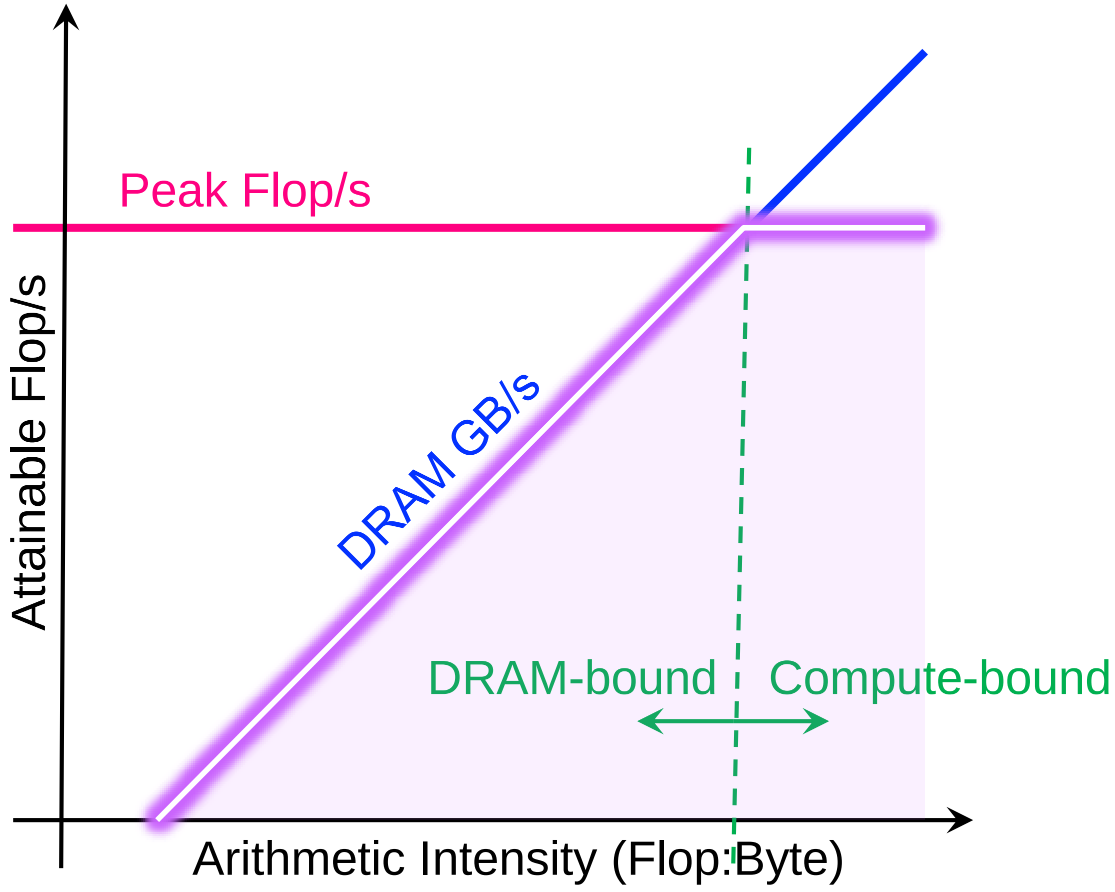


$$\textbf{GFlop/s} = \textbf{min}\begin{cases}\textbf{Peak GFlop/s}\\ \textbf{AI * Peak GB/s}\end{cases}$$

Note, Arithmetic Intensity (AI) = Flops / Bytes (as presented to DRAM)

(DRAM) Roofline

- Plot Roofline bound using Arithmetic Intensity as the x-axis
- **Log-log scale** makes it easy to doodle, extrapolate performance along Moore's Law, etc…
- Kernels with AI less than machine balance are ultimately DRAM bound (we'll refine this later…)



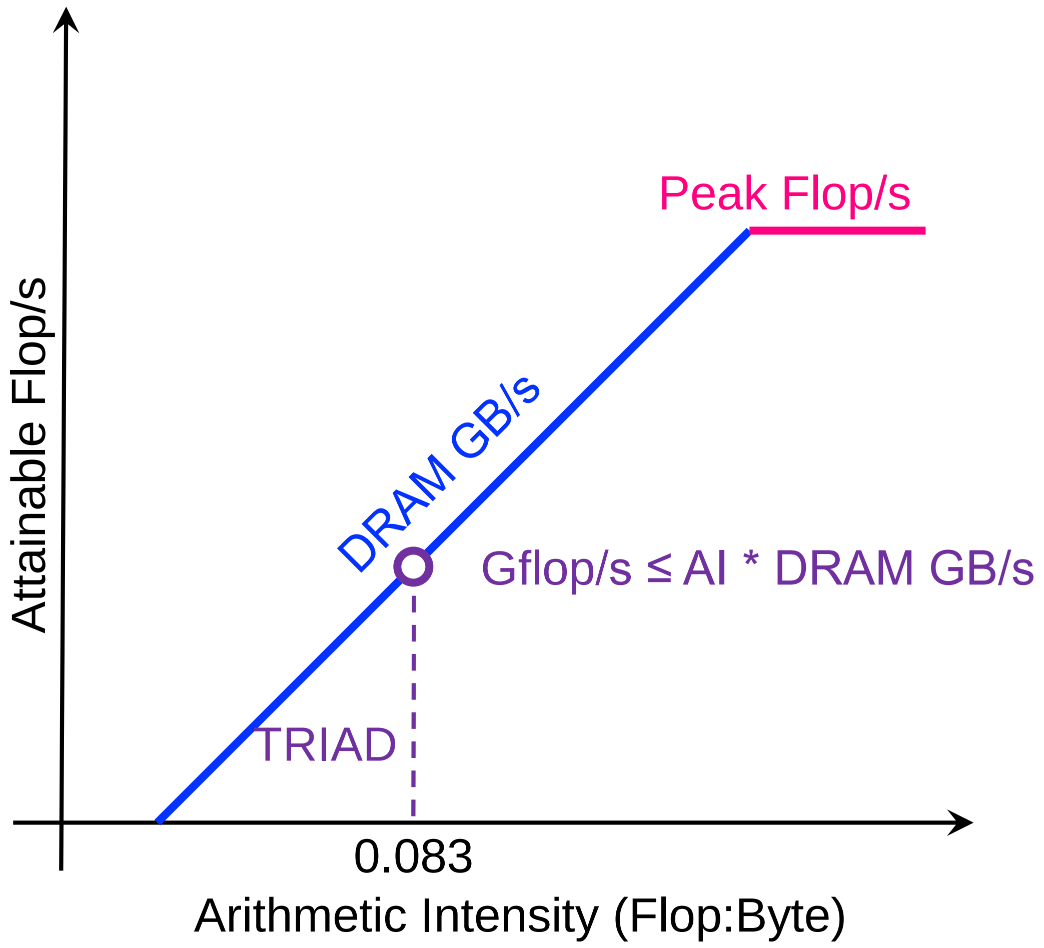
Roofline Example #1

- Typical machine balance is 5-10 flops per byte…
  - 40-80 flops per double to exploit compute capability
  - Artifact of technology and money
  - **Unlikely to improve**

- Consider STREAM Triad…

```
#pragma omp parallel for
for(i=0;i<N;i++){
  Z[i] = X[i] + alpha*Y[i];
}
```

  - 2 flops per iteration
  - Transfer 24 bytes per iteration (read X[i], Y[i], write Z[i])
  - **AI = 0.083 flops per byte == Memory bound**



Roofline Example #2

- Conversely, 7-point constant coefficient stencil…
  - 7 flops
  - 8 memory references (7 reads, 1 store) per point
  - Cache can filter all but 1 read and 1 write per point
  - **AI = 0.44 flops per byte == memory bound, but 5x the flop rate**

```
#pragma omp parallel for
for(k=1;k<dim+1;k++){
for(j=1;j<dim+1;j++){
for(i=1;i<dim+1;i++){
  new[k][j][i] = -6.0*old[k  ][j  ][i  ]
                    + old[k  ][j  ][i-1]
                    + old[k  ][j  ][i+1]
                    + old[k  ][j-1][i  ]
                    + old[k  ][j+1][i  ]
                    + old[k-1][j  ][i  ]
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}}}
```
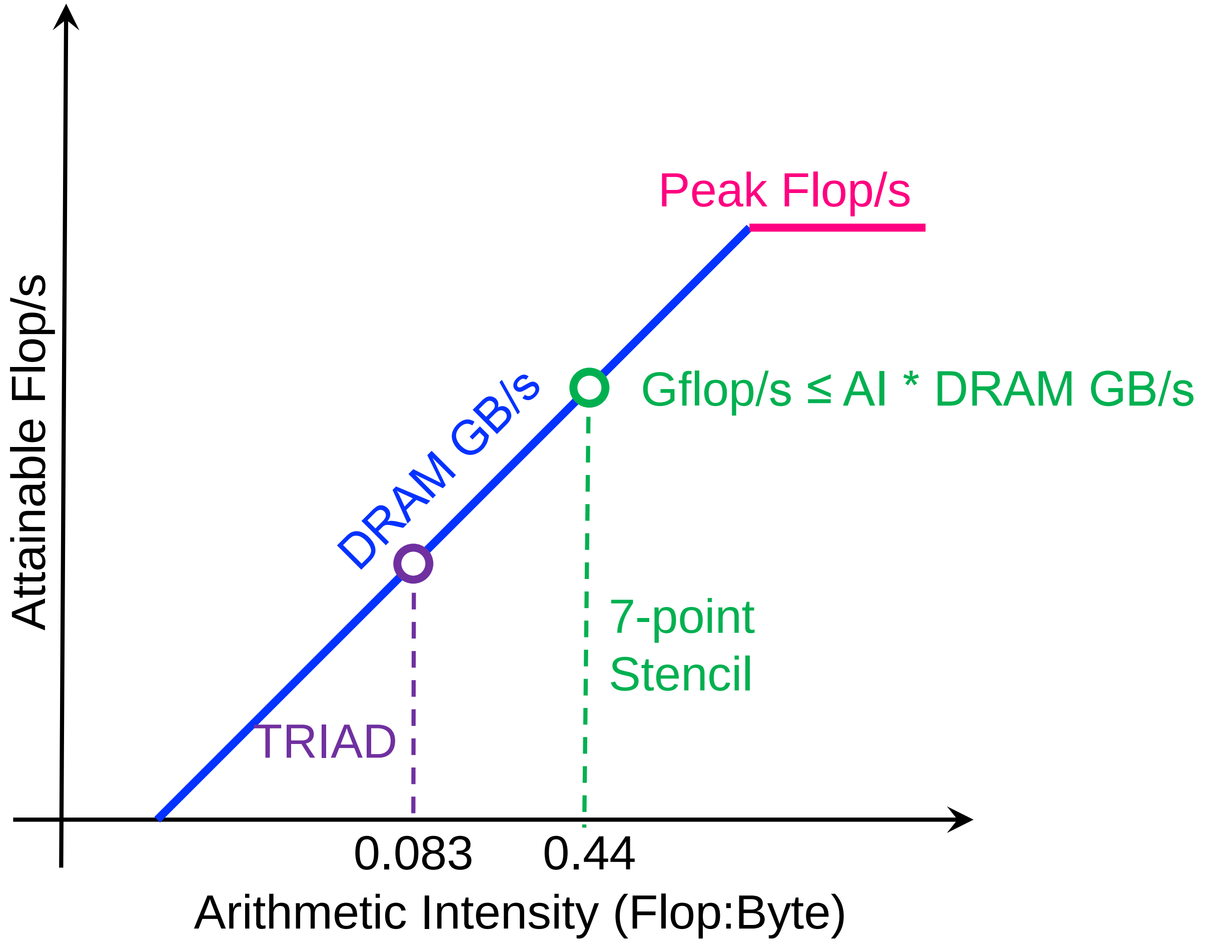
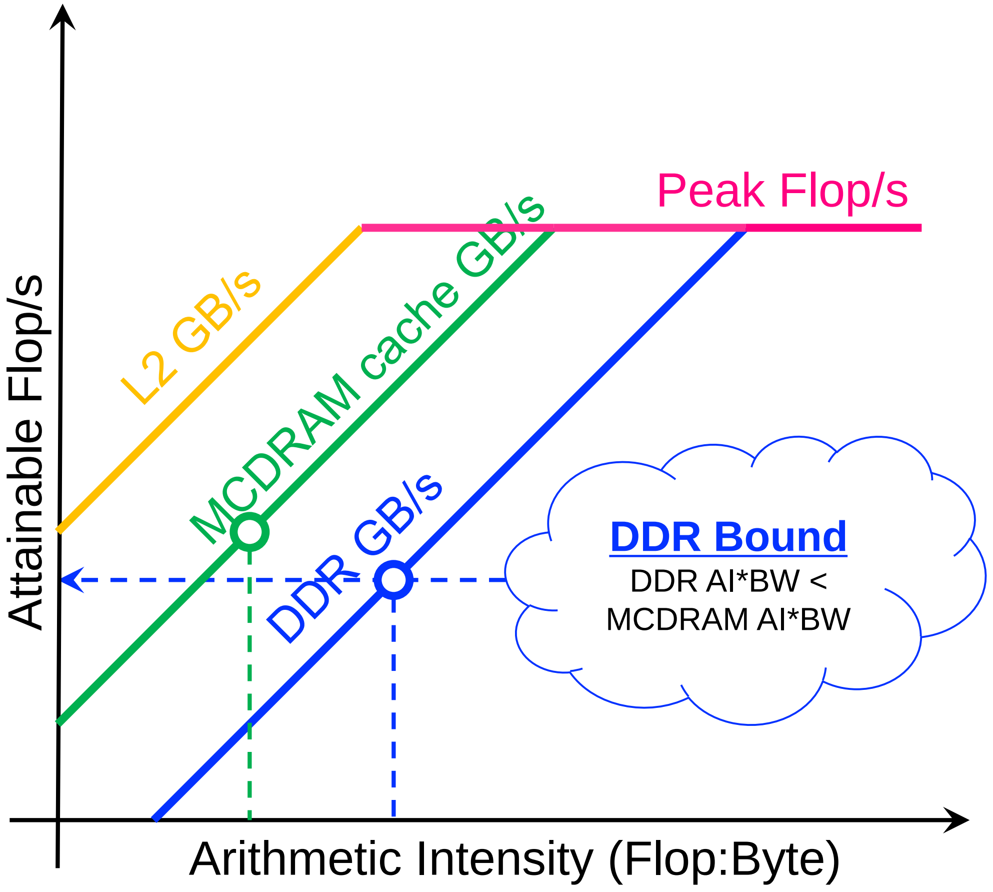



Hierarchical Roofline

- Real processors have multiple levels of memory
  - Registers
  - L1, L2, L3 cache
  - MCDRAM/HBM (KNL/GPU device memory)
  - DDR (main memory)
  - NVRAM (non-volatile memory)
- Applications can have locality in each level
  - Unique data movements imply unique AI’s
  - Moreover, each level will have a unique bandwidth

Hierarchical Roofline

- Construct superposition of Rooflines…
  - Measure a bandwidth
  - Measure AI for each level of memory
  - Although an loop nest may have multiple AI's and multiple bounds (flops, L1, L2, … DRAM)…
  - **… performance is bound by the minimum**



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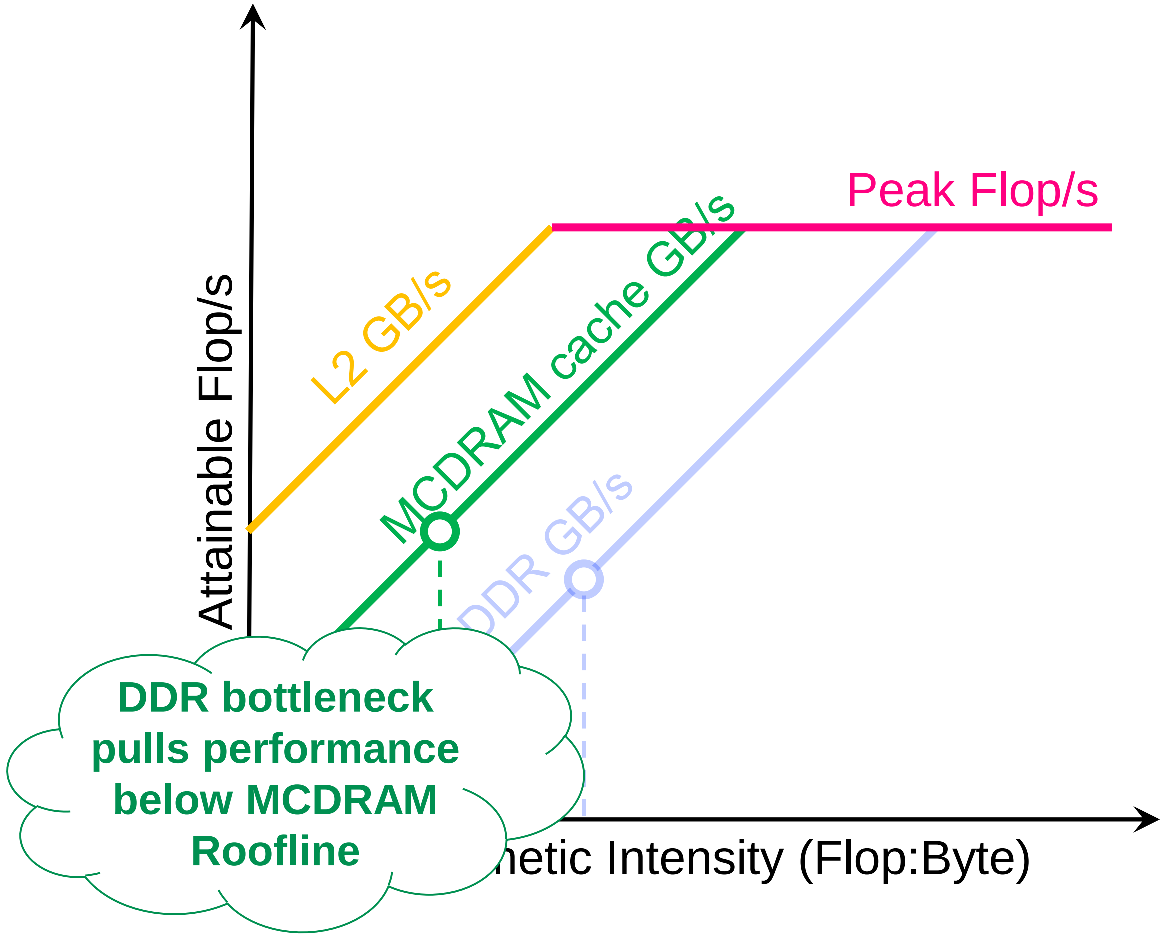

DDR bottleneck pulls performance below MCDRAM Roofline

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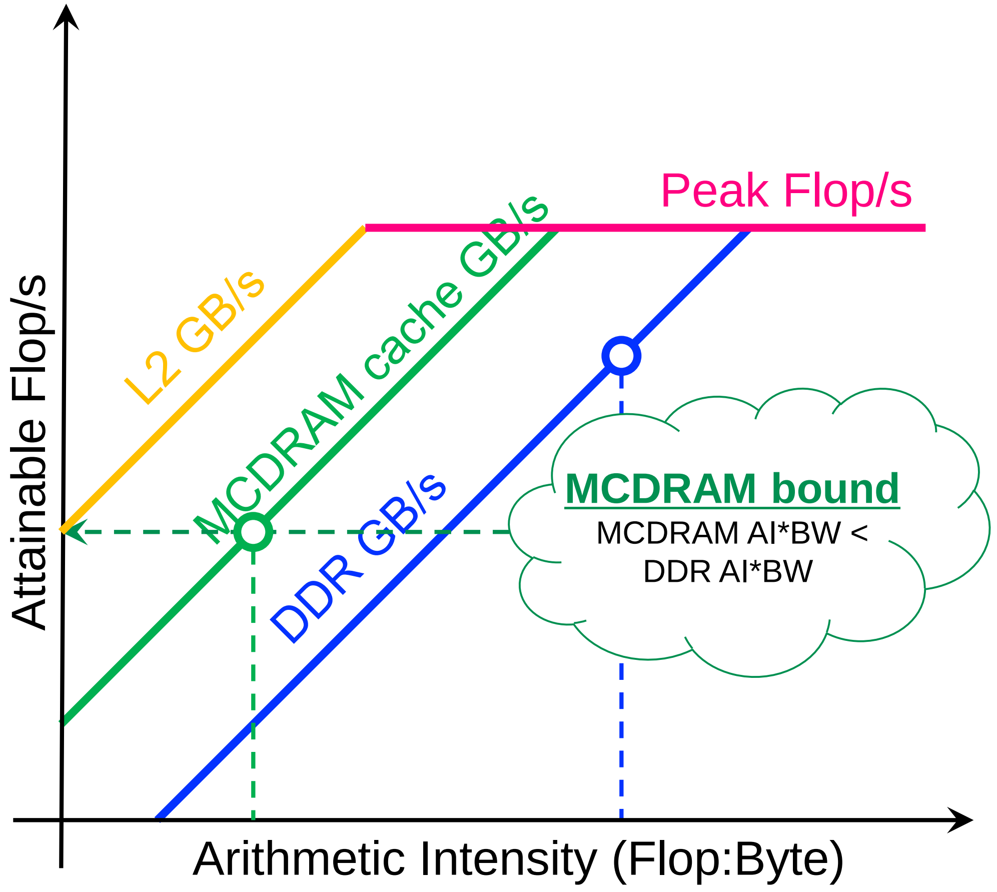

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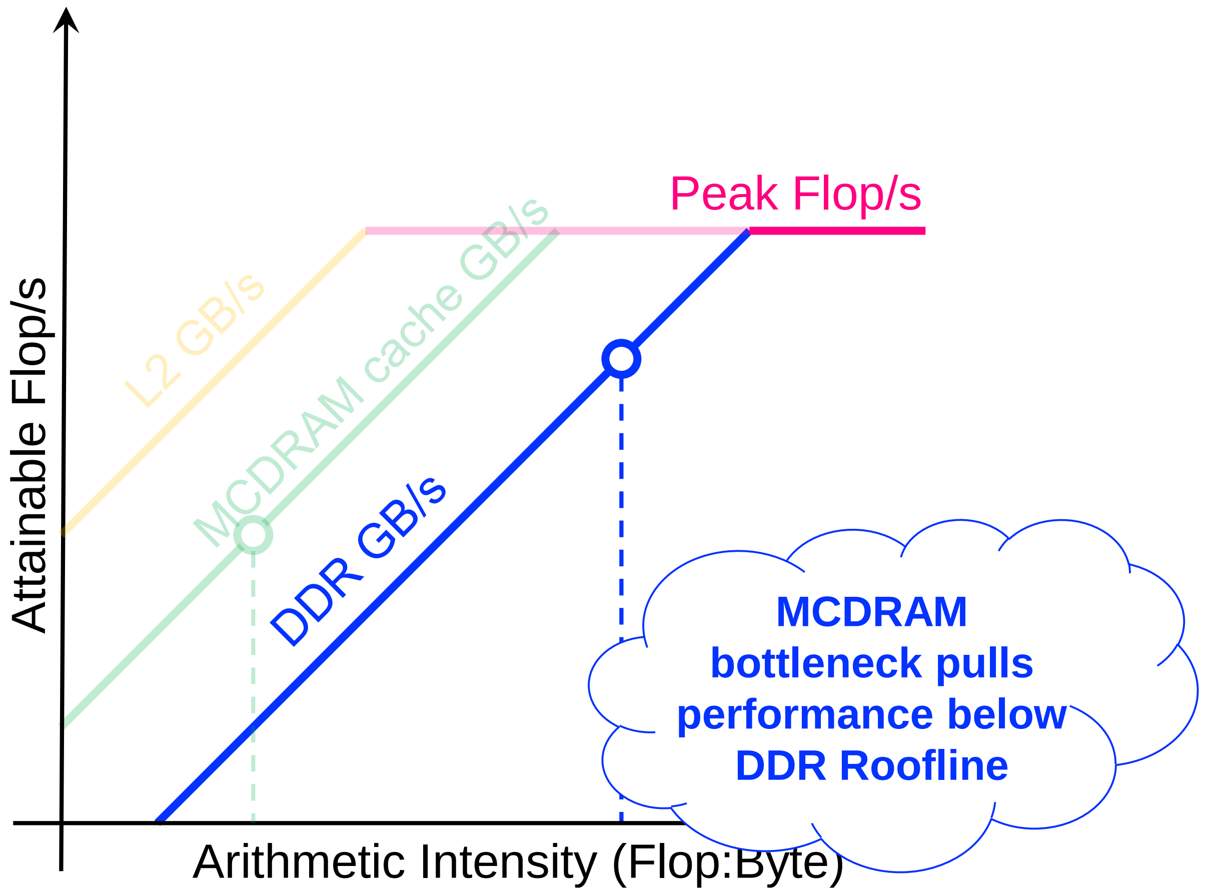
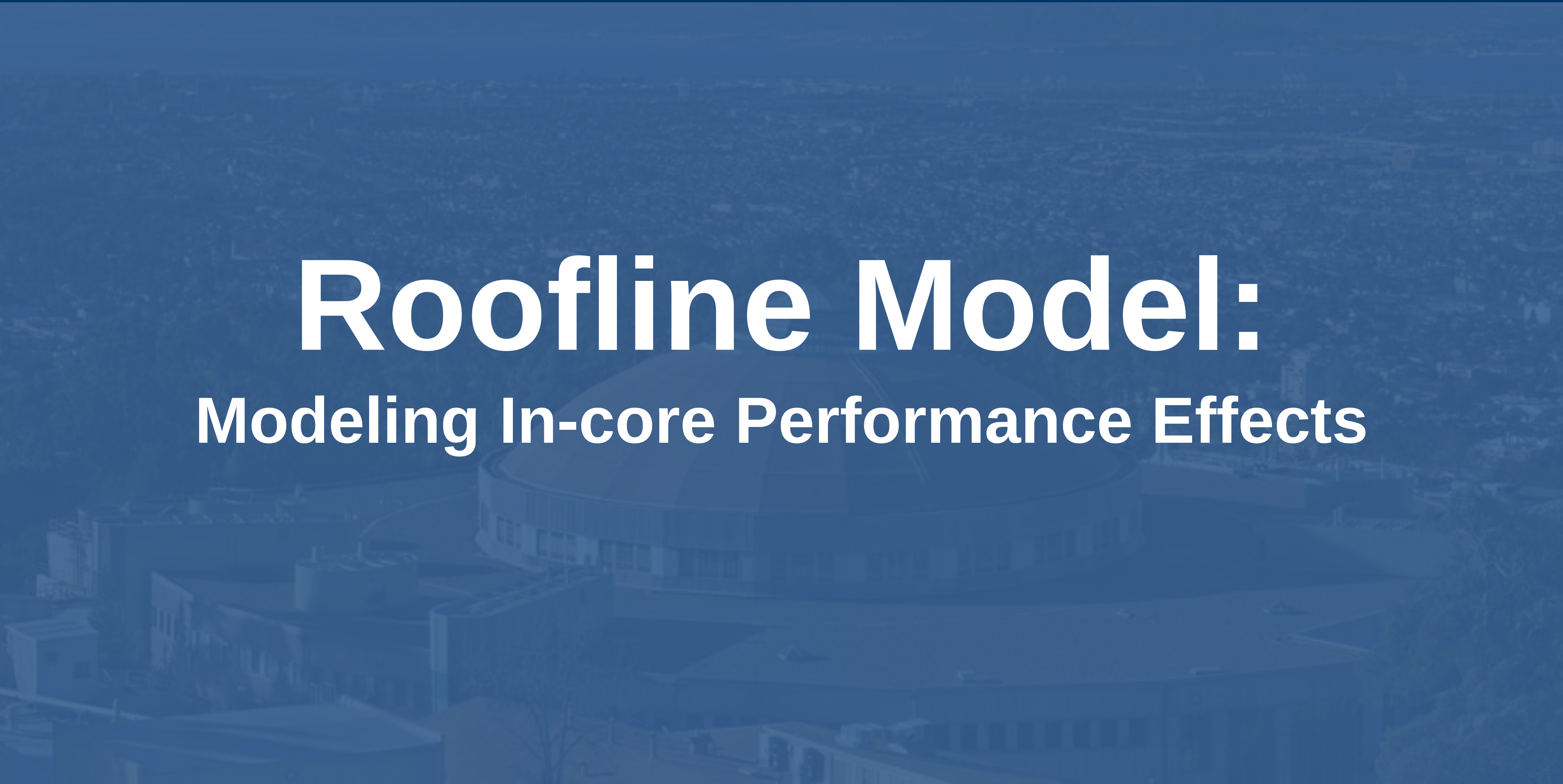


MCDRAM bottleneck pulls performance below DDR Roofline



Roofline Model:

Modeling In-core Performance Effects

Data, Instruction, Thread-Level Parallelism…

- Modern CPUs use several techniques to increase per core Flop/s

Fused Multiply Add

- w = x*y + z is a common idiom in linear algebra
- Ra er ving se d a se a add (FMA)
- Th U chains the multiply and add in a single pipeline so that it can complete FMA/cycle

Resurgence… Tensor Cores, QFMA, etc… !

Vector Instructions

- Many HPC codes apply the same operation to a vector of elements
- Vendors provide vector instructions that apply the same operation to 2, 4, 8, 16 elements…

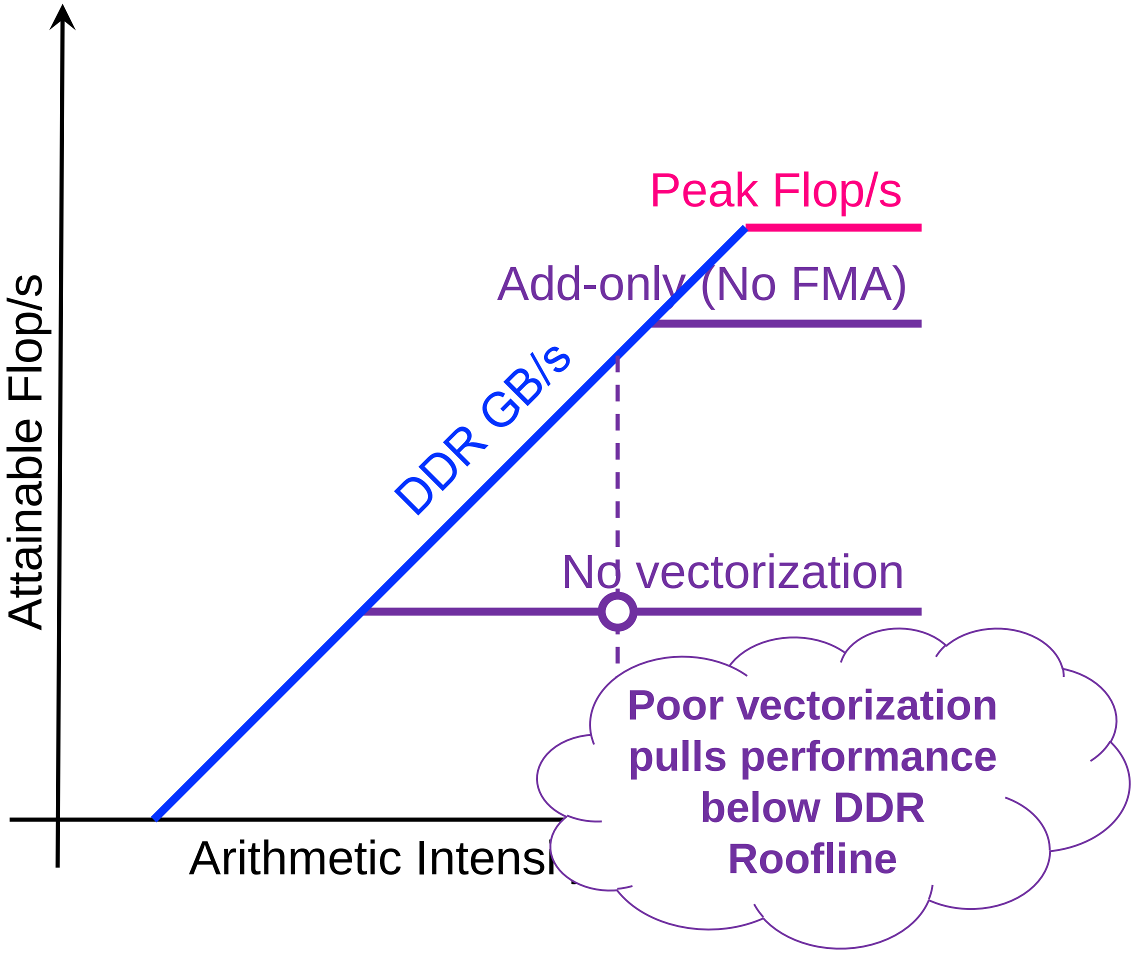
  x [0:7] *y [0:7] + z [0:7]
- Vector FPUs complete 8 vector operations/cycle

Deep pipelines

- The hardware for a FMA is substantial.
- Breaking a single FMA up into several smaller operations and pipelining them allows vendors to increase GHz
- Little’s Law applies… need FP_Latency * FP_bandwidth independent instructions

Data, Instruction, Thread-Level Parallelism…

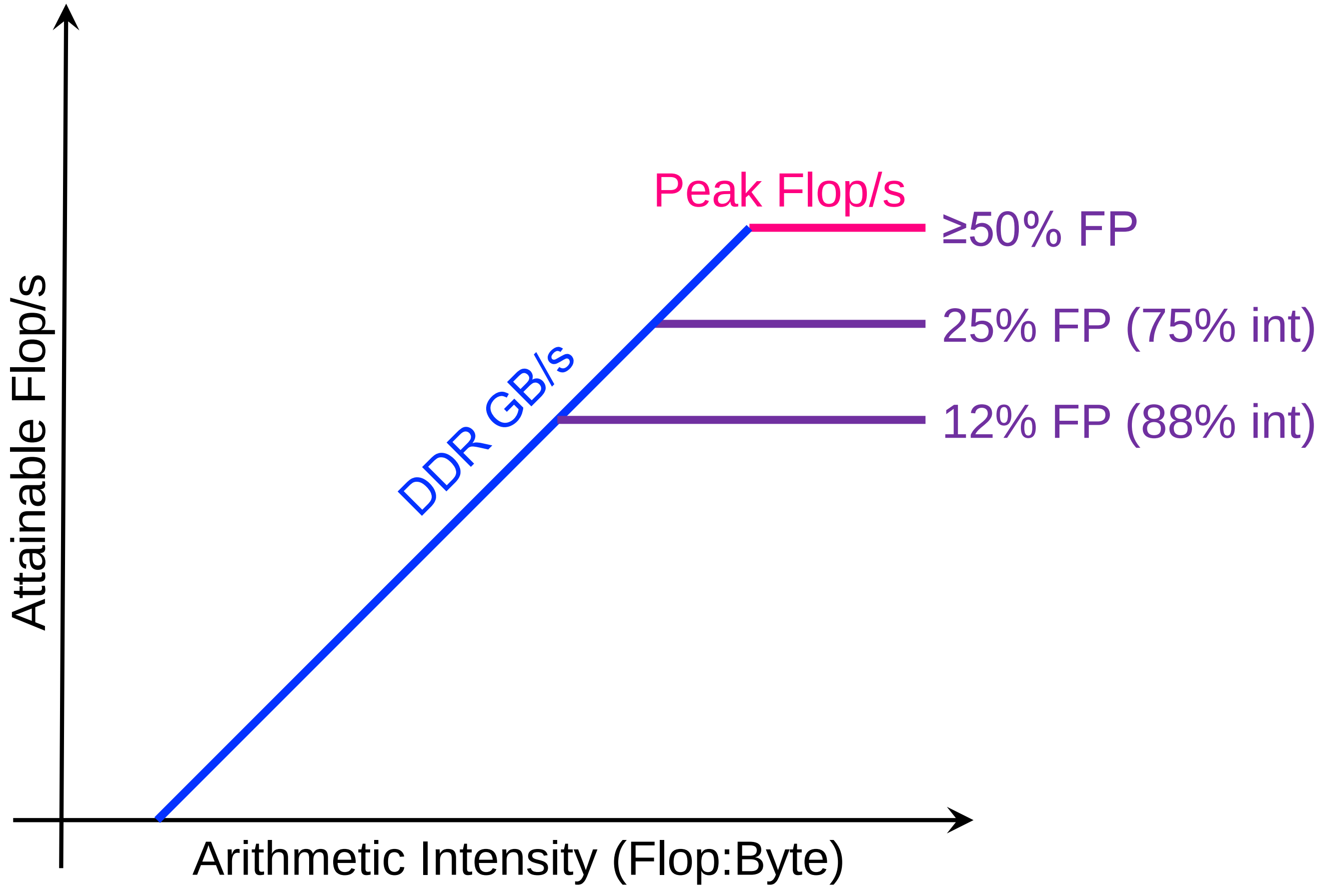
- If every instruction were an ADD (instead of FMA), **performance would drop by 2x on KNL or 4x on Haswell**
- Similarly, if one failed to vectorize, performance would drop by **another 8x on KNL and 4x on Haswell**
- Lack of threading (or load imbalance) will reduce performance by another 64x on KNL.



Poor vectorization pulls performance below DDR Roofline

Superscalar vs. Instruction mix

- Define in-core ceilings based on instruction mix…
- e.g. Haswell
  - 4-issue superscalar
  - Only 2 FP data paths
  - Requires 50% of the instructions to be FP to get peak performance



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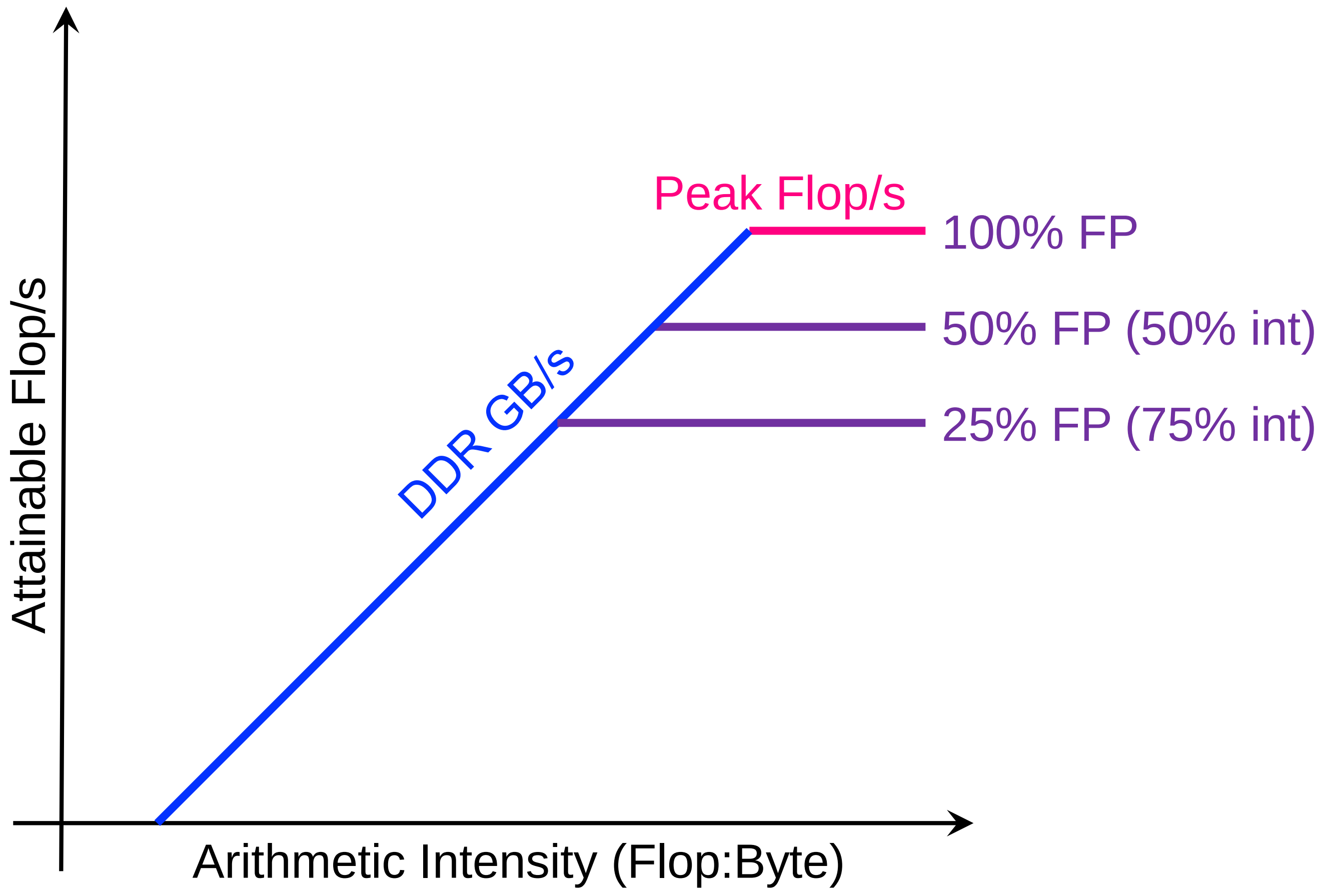

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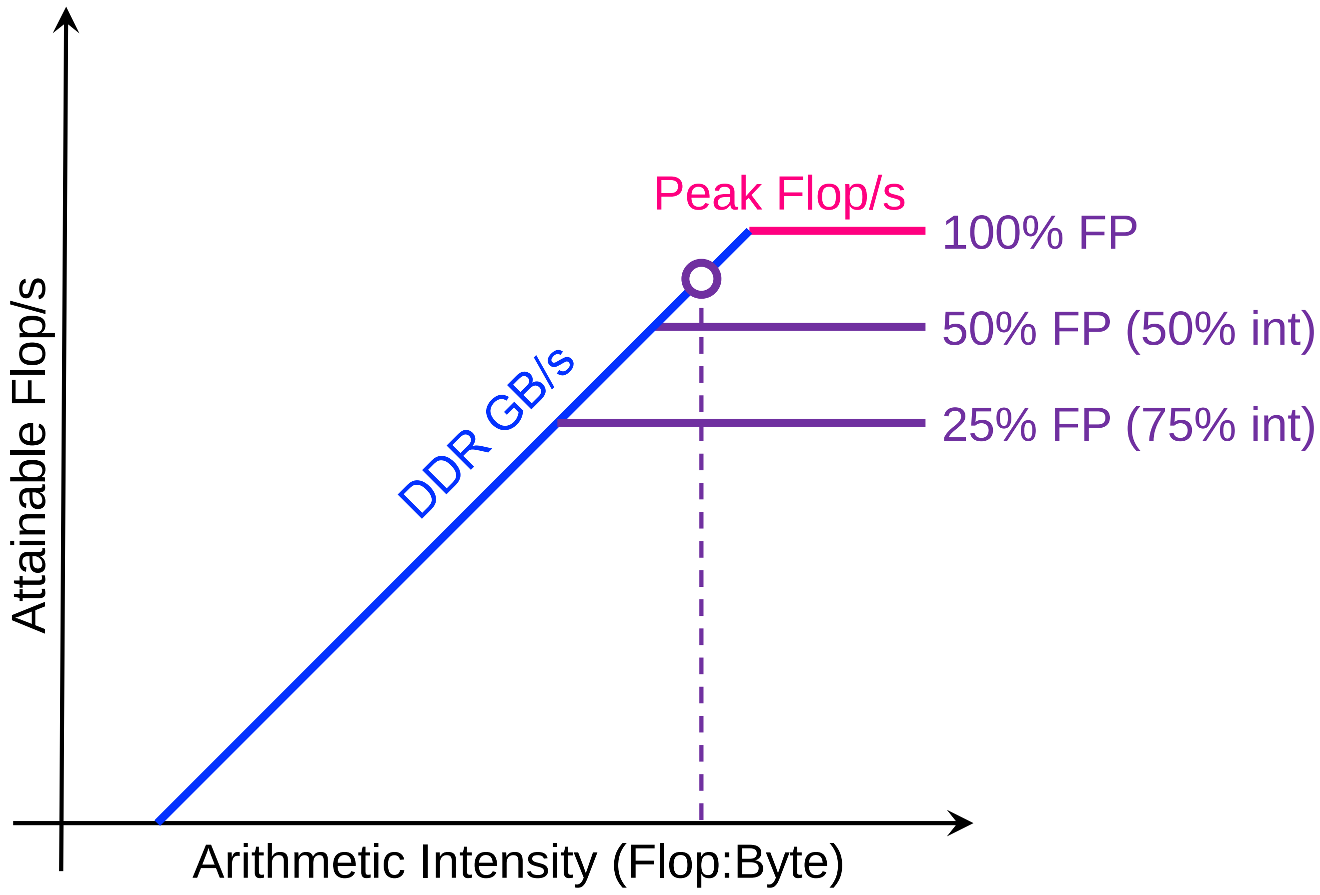

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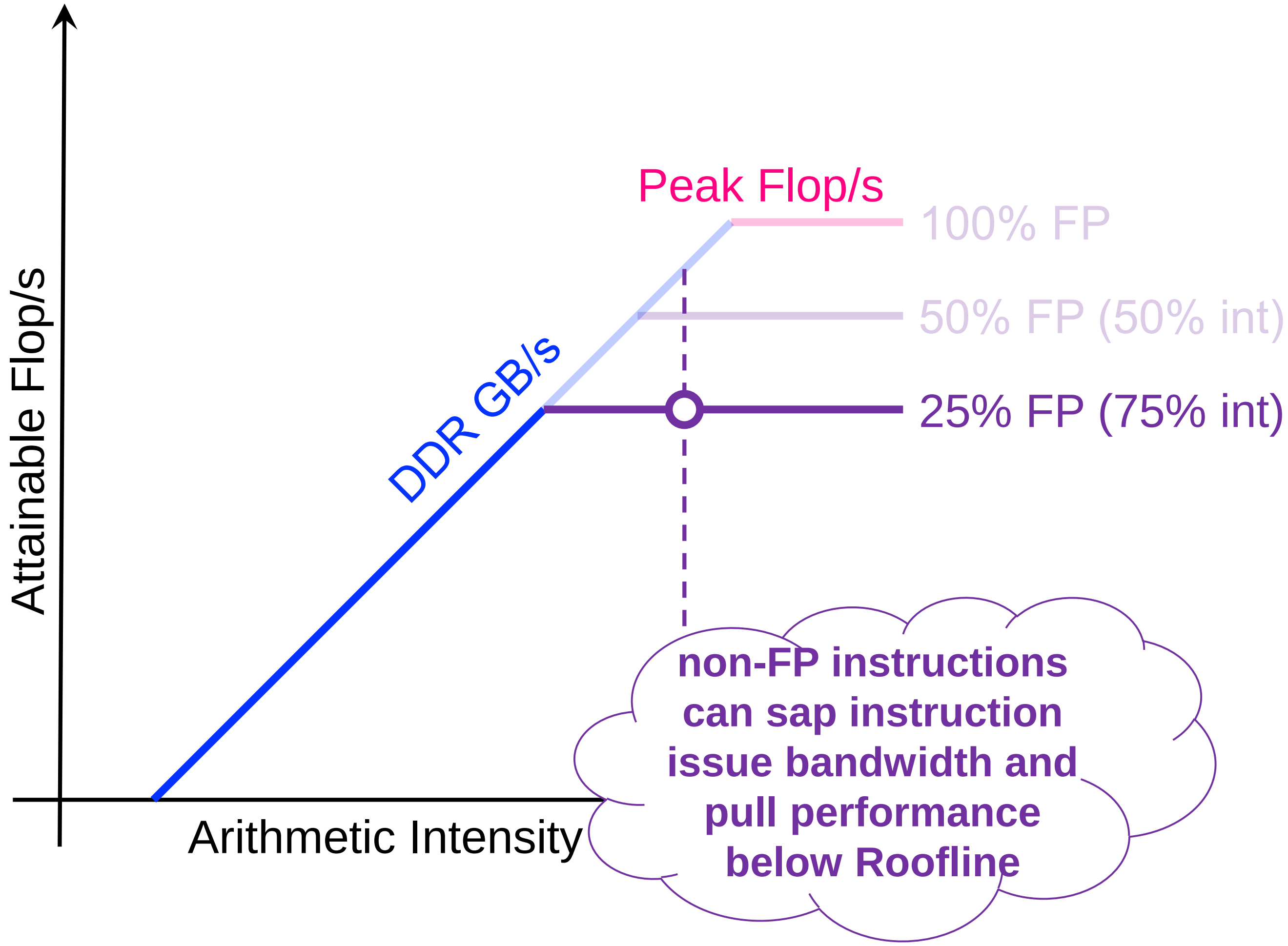
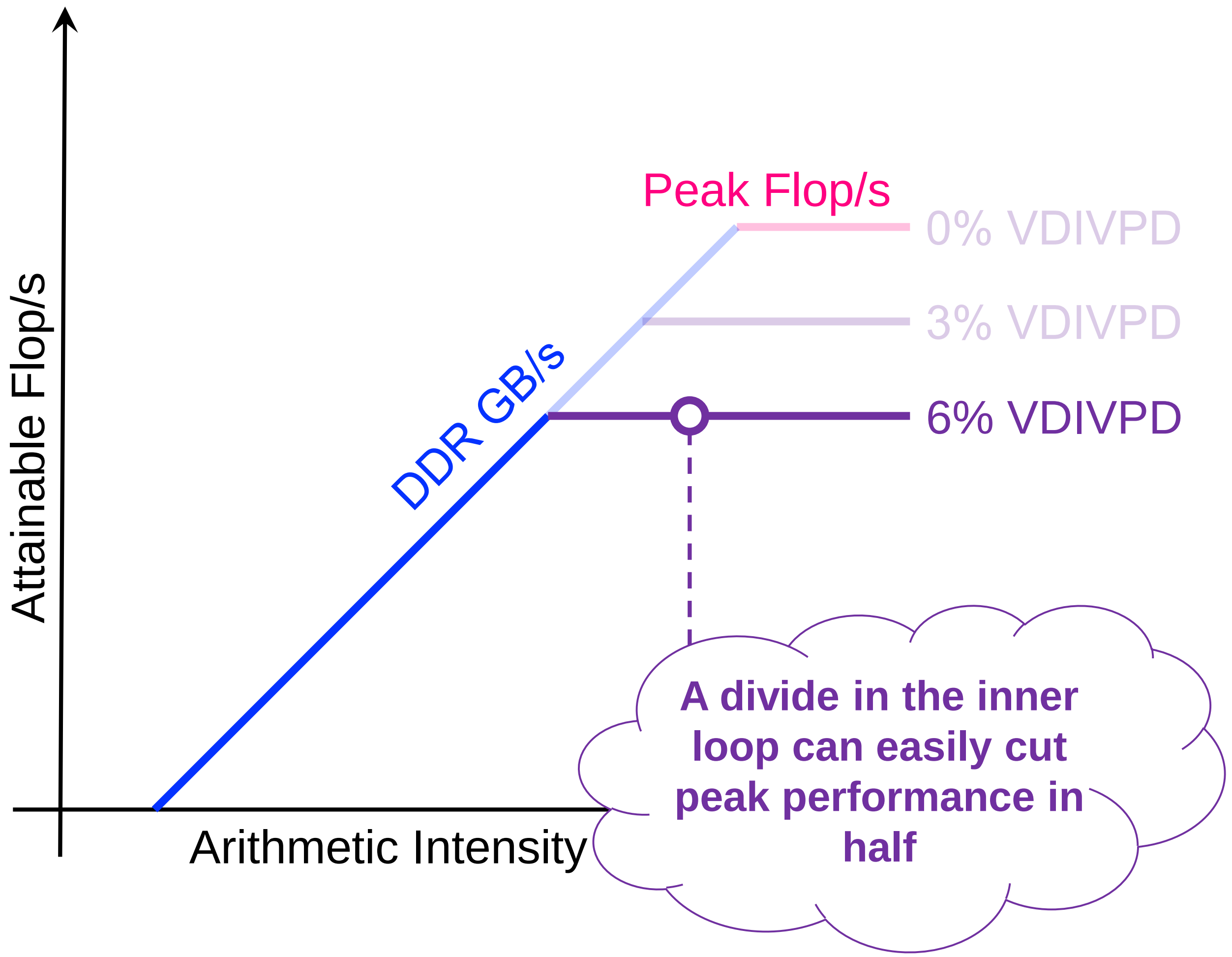


non-FP instructions can sap instruction issue bandwidth and pull performance below Roofline

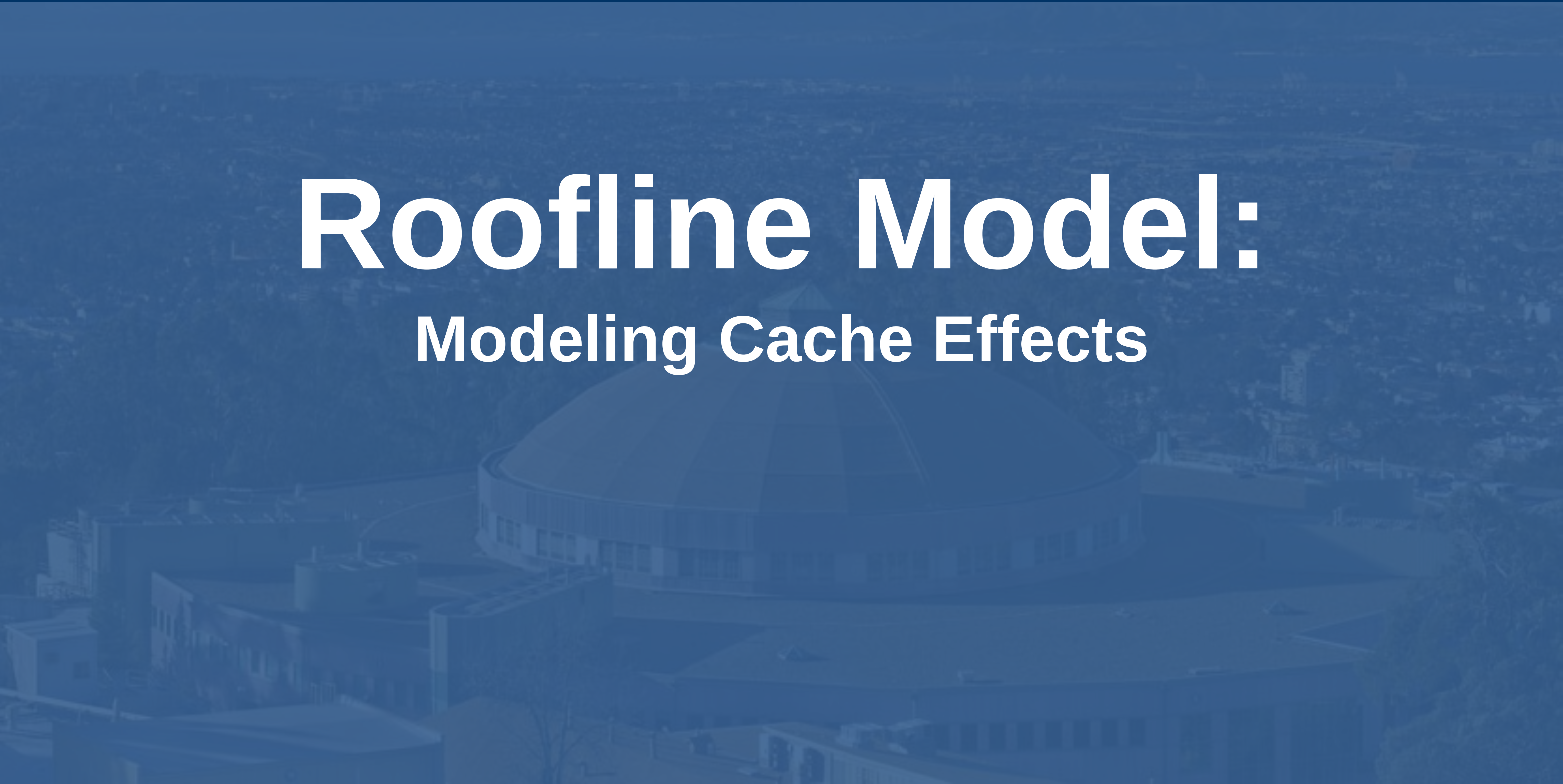
Divides and other Slow FP instructions

- FP Divides (sqrt, rsqrt, …) might support only limited pipelining
- As such, their throughput is substantially lower than FMA's
- If divides constitute even if 3% of the flop's come from divides, performance can be cut in half.

➢ *Penalty varies substantially between architectures and generations (e.g. IVB, HSW, KNL, …)*



A divide in the inner loop can easily cut peak performance in half

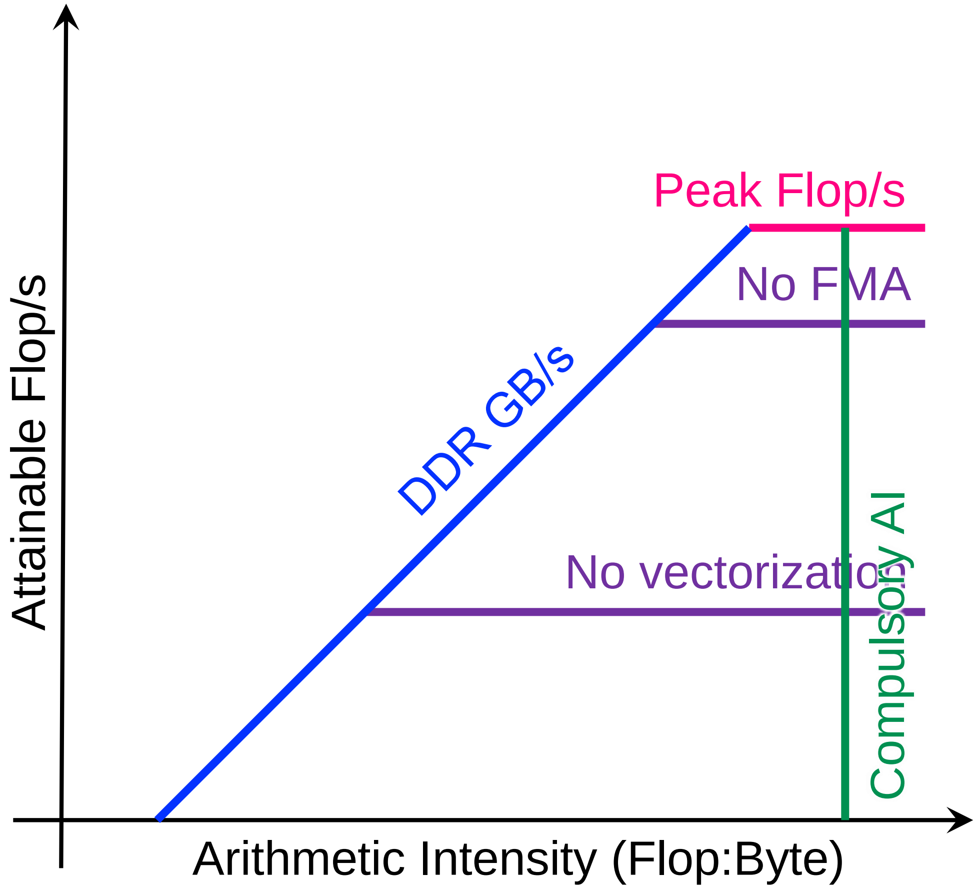


Roofline Model:

Modeling Cache Effects

Locality Walls

- Naively, we can bound AI using only compulsory cache misses



$$\text{AI} = \frac{\#\text{Flop's}}{\text{Compulsory Misses}}$$

Locality Walls

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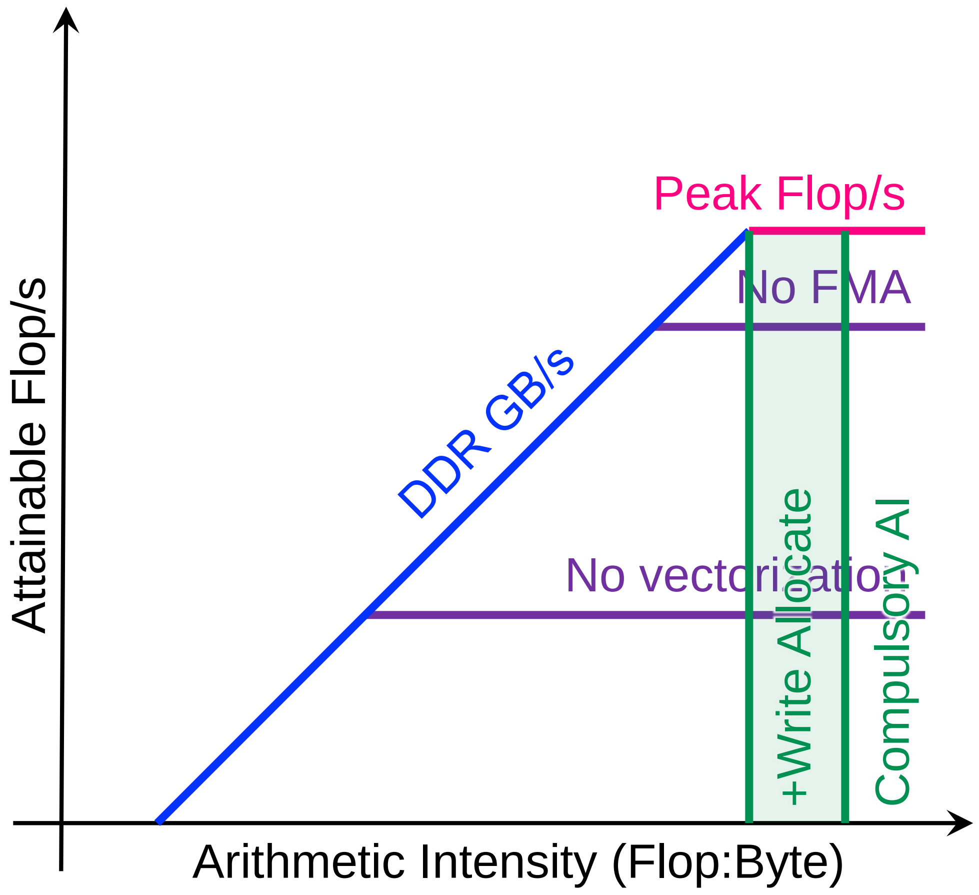
- However, write allocate caches can lower AI



$$AI = \frac{\#Flop's}{\text{Compulsory Misses + Write Allocates}}$$

Locality Walls

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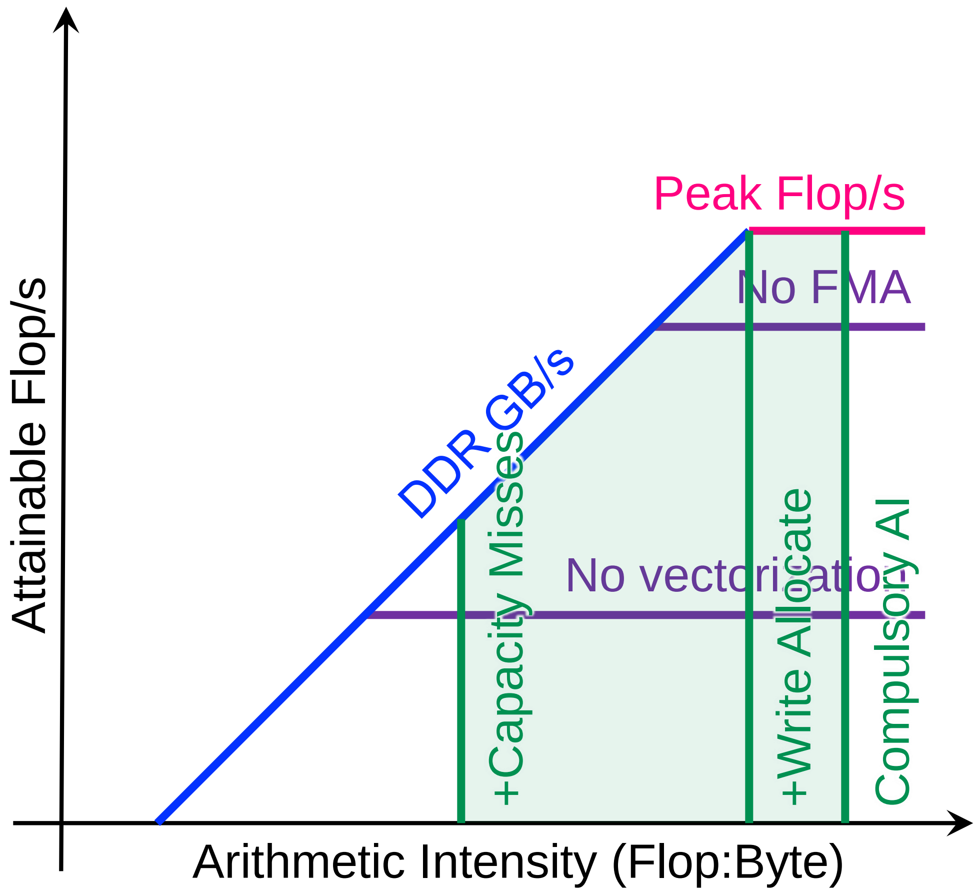
- However, write allocate caches can lower AI
- Cache capacity misses can have a huge penalty



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Locality Walls

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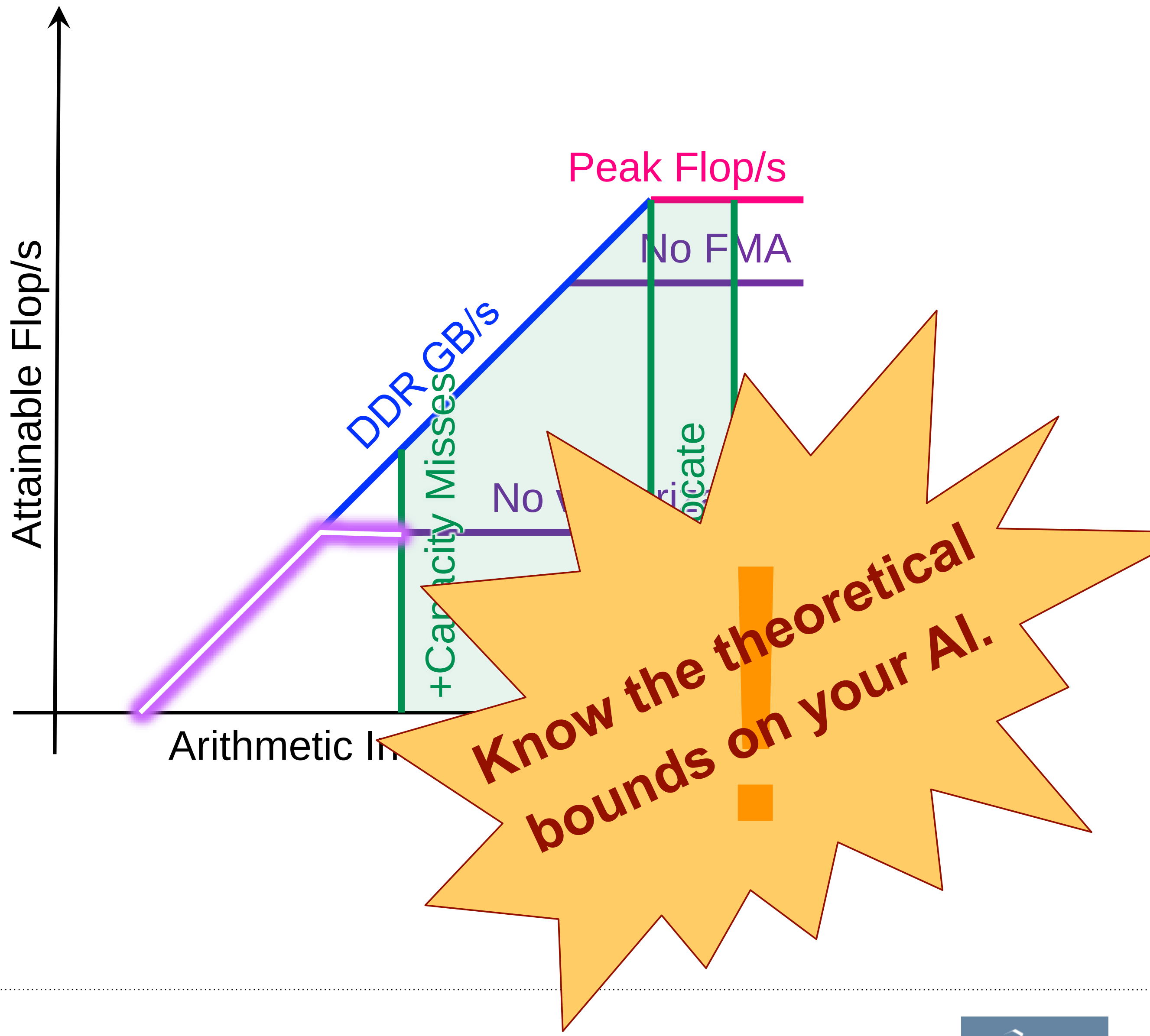
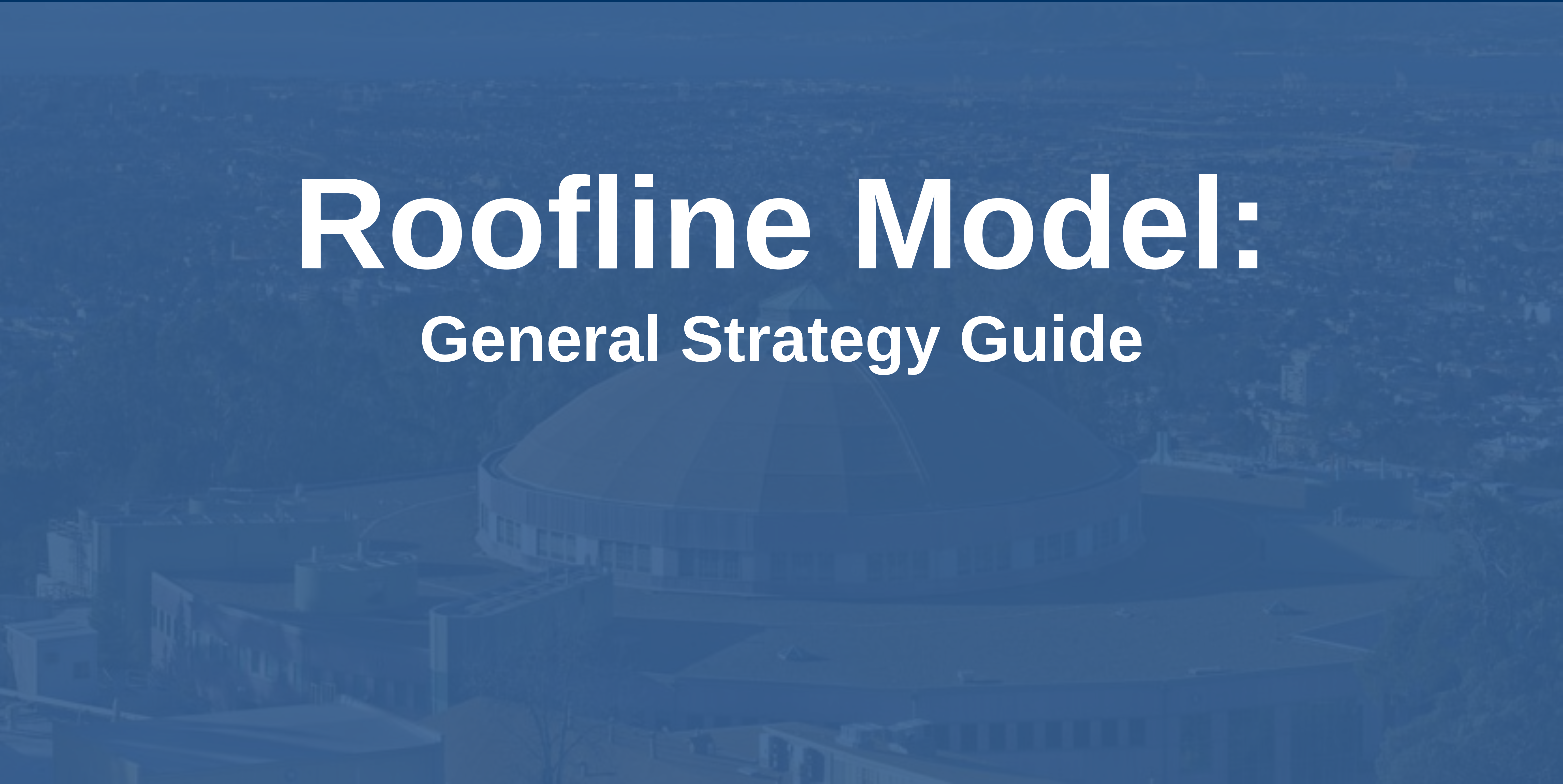
➢ **Compute bound became memory bound**

$$\text{AI} = \frac{\text{\#Flop's}}{\text{Compulsory Misses + Write Allocates + Capacity Misses}}$$



Know the theoretical bounds on your AI.

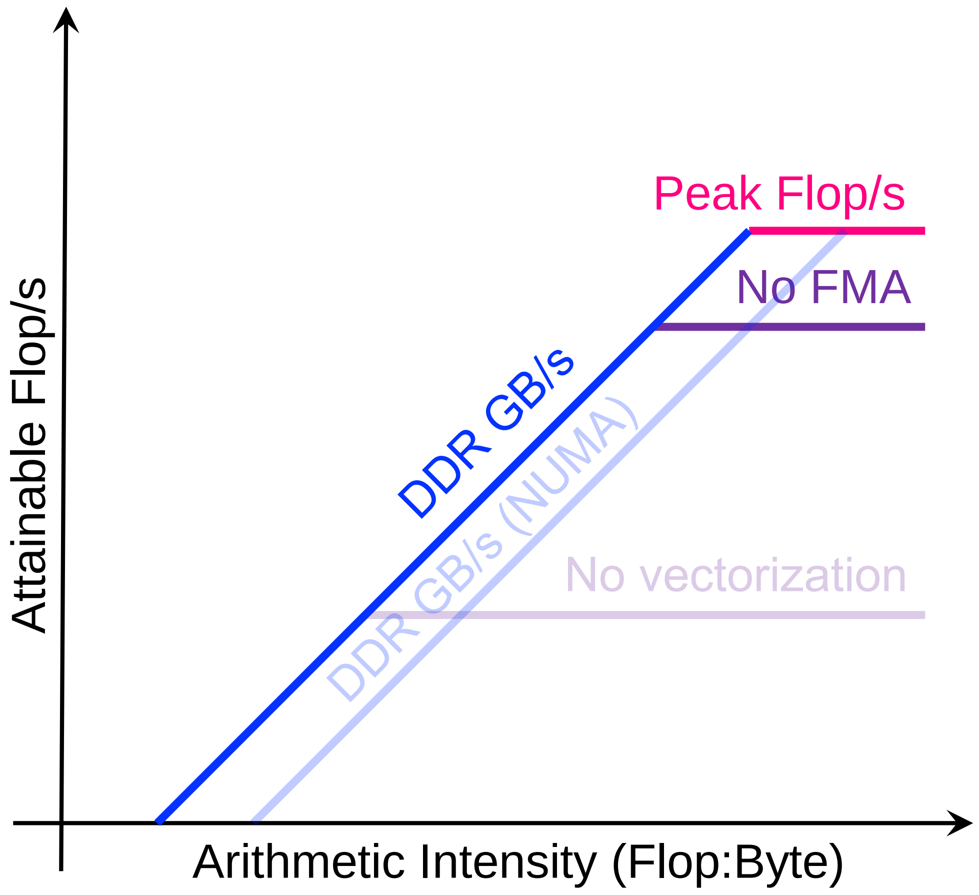


Roofline Model:

General Strategy Guide

General Strategy Guide

- Broadly speaking, there are three approaches to improving performance:



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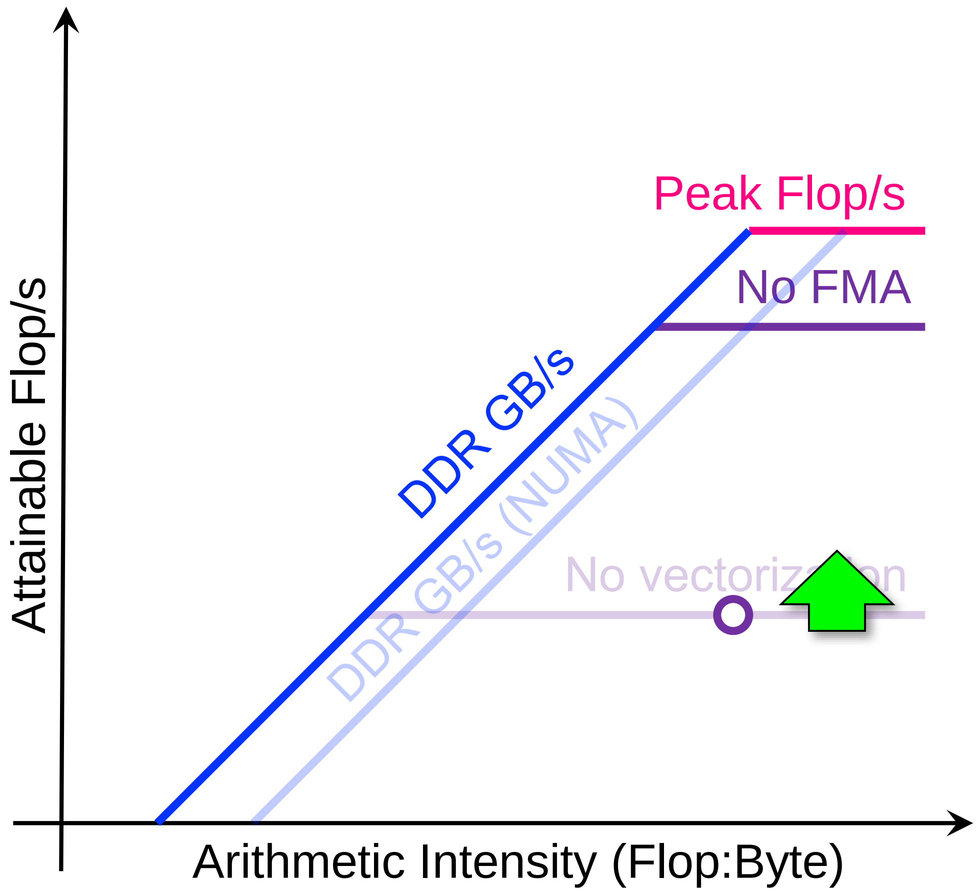
- **Maximize in-core performance (e.g. get compiler to vectorize)**



General Strategy Guide

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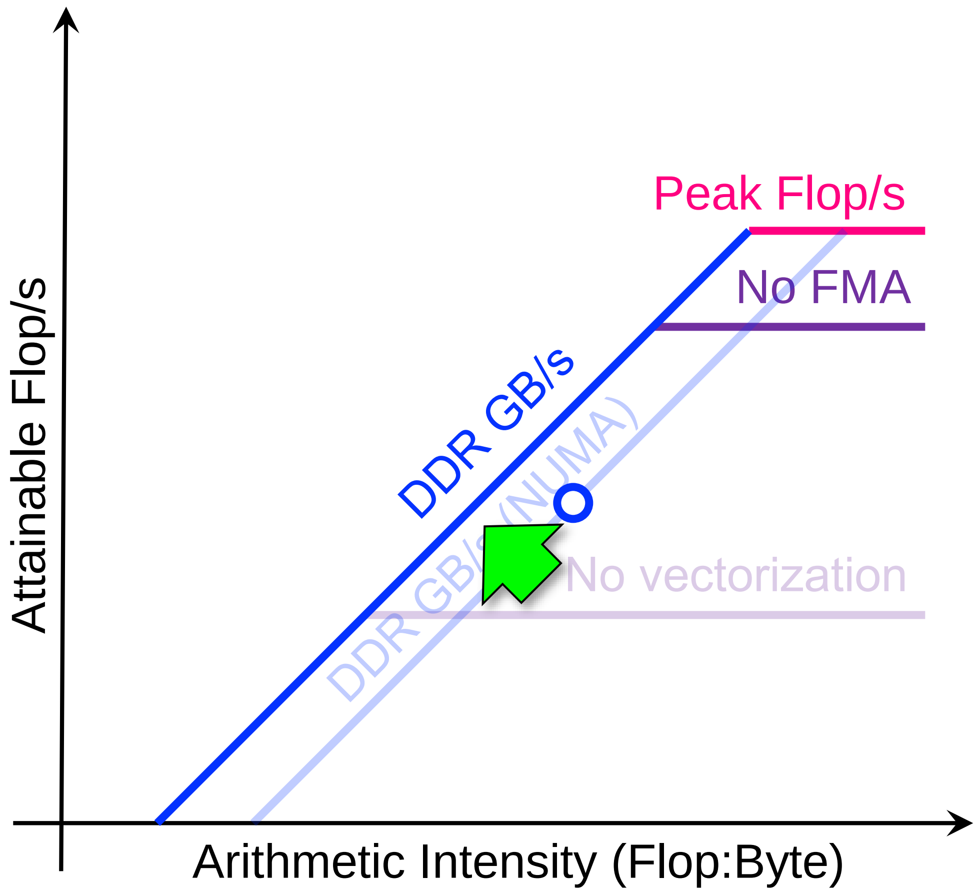
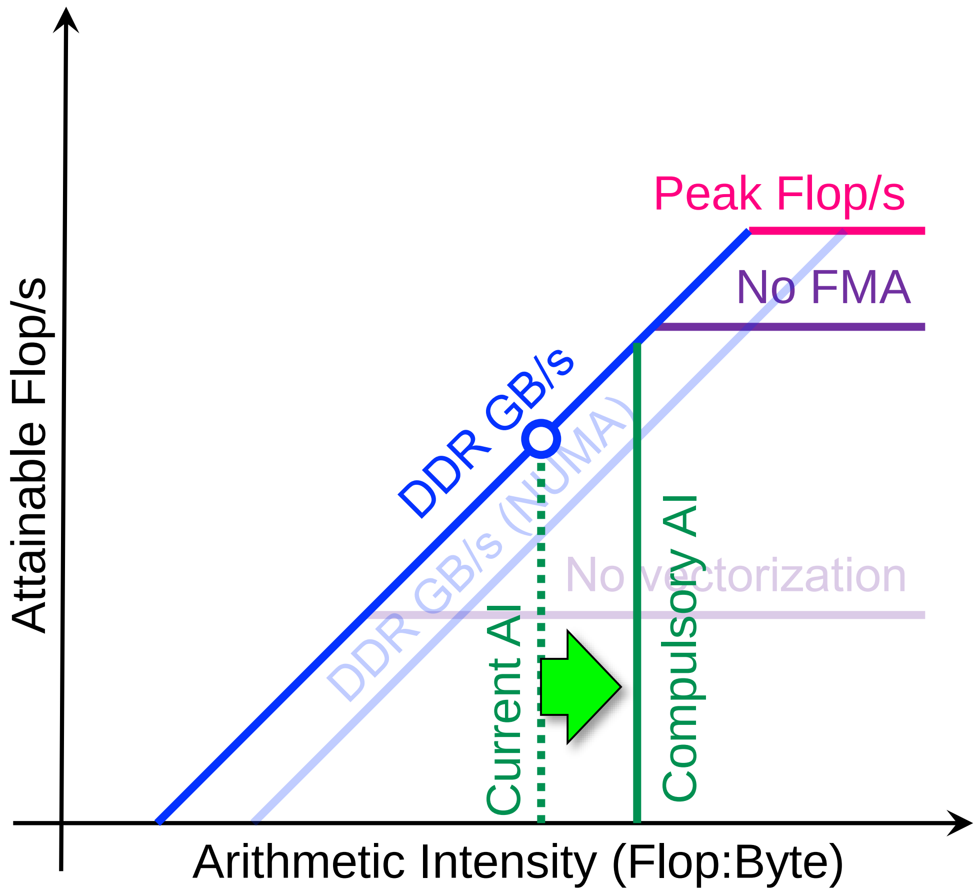
- **Maximize memory bandwidth (e.g. NUMA-aware allocation)**



General Strategy Guide

- Broadly speaking, there are three approaches to improving performance:
- Maximize in-core performance (e.g. get compiler to vectorize)
- Maximize memory bandwidth (e.g. NUMA-aware allocation)
- **Minimize data movement (increase AI)**



Constructing a Roofline Model requires answering some questions…

Questions can overwhelm users…

Properties of the target machine

(Benchmarking)

What is my machine's peak flop/s?

How important is vectorization or FMA on my machine?

What is my machine's DDR GB/s?

L2 GB/s?

Properties of an application's execution

(Instrumentation)

How much data did my kernel actually move?

Did my kernel vectorize?

How many flop's did my kernel actually do?

How much did that divide hurt?

Fundamental properties of the kernel constrained by hardware

(Theory)

What is my kernel's compulsory AI?

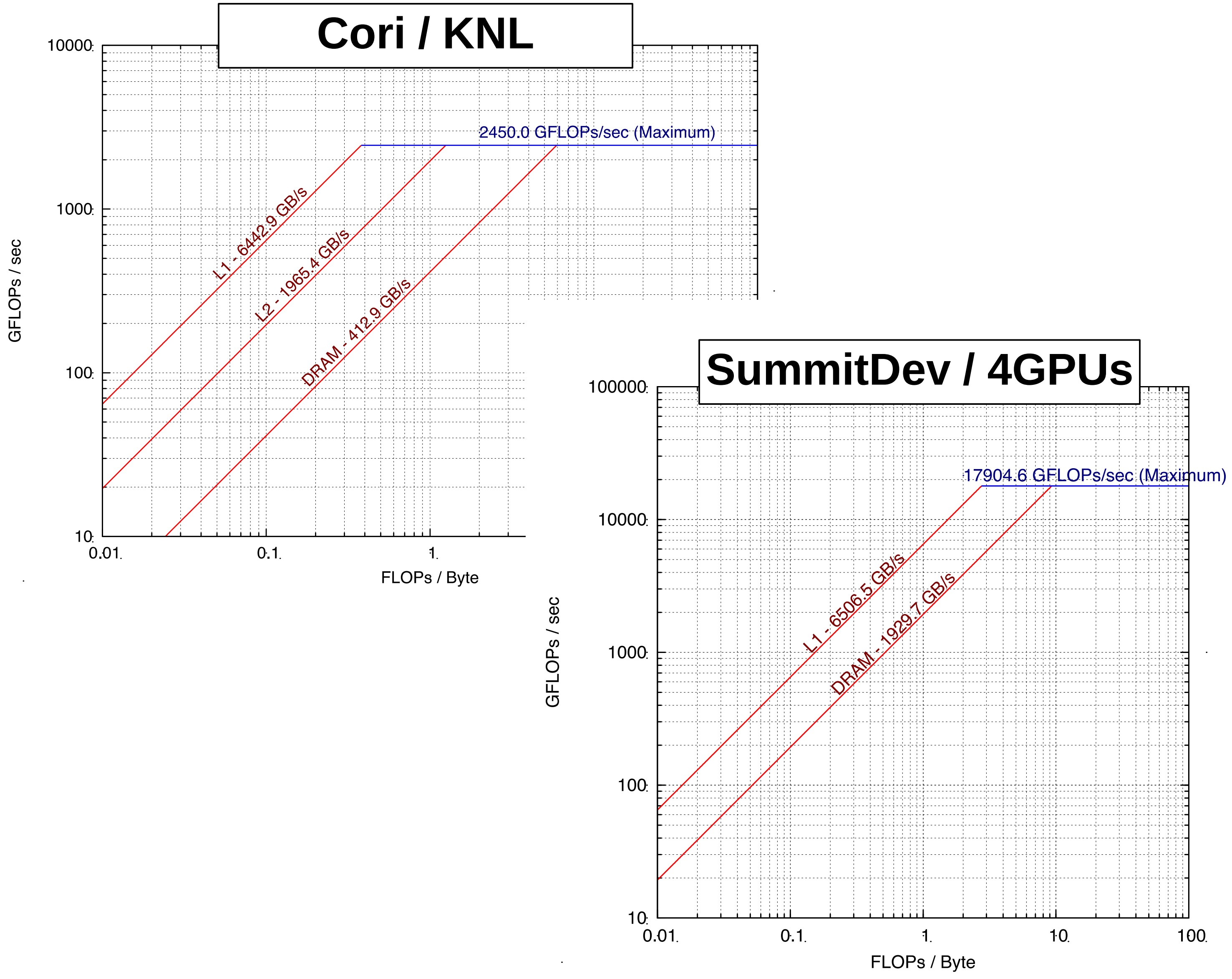
(communication lower bounds)

Can my kernel ever be vectorized?

We need tools…

Node Characterization?

- **“Marketing Numbers”** can be deceptive…
  - Pin BW vs. real bandwidth
  - TurboMode / Underclock for AVX
  - compiler failings on high-AI loops.
- LBL developed the Empirical Roofline Toolkit (ERT)…
  - Characterize CPU/GPU systems
  - Peak Flop rates
  - Bandwidths for each level of memory
  - **MPI+OpenMP/CUDA == multiple GPUs**



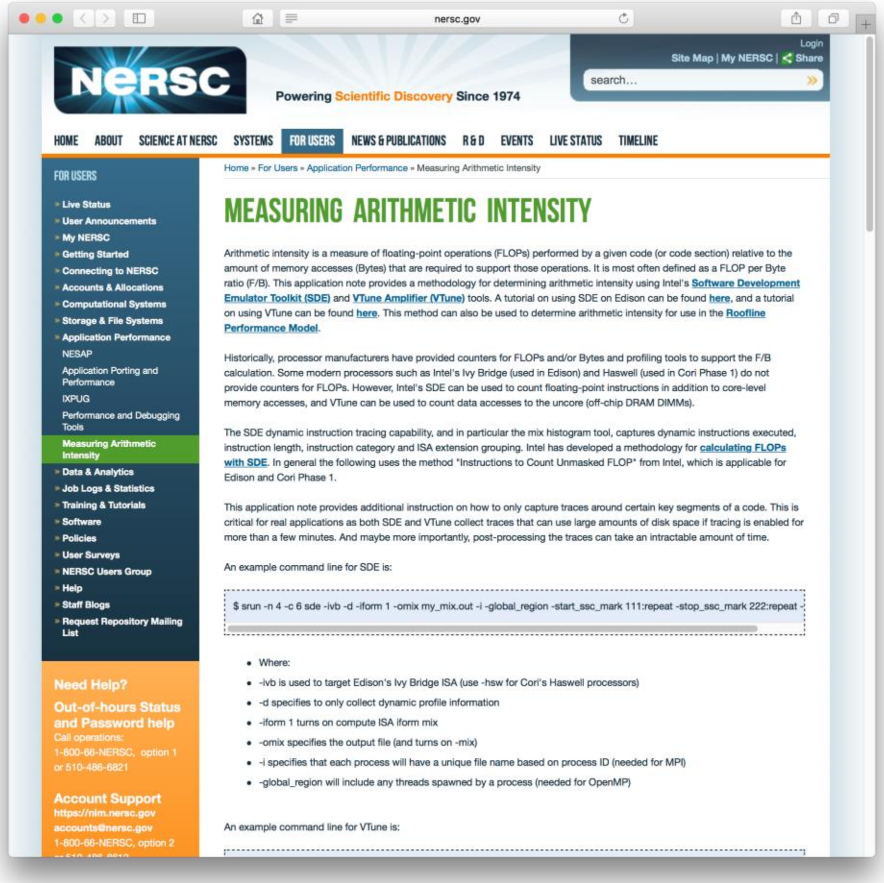
https://crd.lbl.gov/departments/computer-science/PAR/research/roofline/

Instrumentation with Performance Counters?

- ***Characterizing applications with performance counters can be problematic…***
  - Flop Counters can be broken/missing in production processors
  - Vectorization/Masking can complicate counting Flop’s
  - Counting Loads and Stores doesn’t capture cache reuse while counting cache misses doesn’t account for prefetchers.
  - DRAM counters (Uncore PMU) might be accurate, but…
    - are privileged and thus nominally inaccessible in user mode
    - may need vendor (e.g. Cray) and center (e.g. NERSC) approved OS/kernel changes

Forced to Cobble Together Tools…

- Use tools known/observed to work on NERSC's Cori (KNL, HSW)…
  - Used **Intel SDE** (Pin binary instrumentation + emulation) to create software Flop counters
  - Used **Intel VTune** performance tool (NERSC/Cray approved) to access uncore counters
- ➢ Accurate measurement of Flop's (HSW) and DRAM data movement (HSW and KNL)
- ➢ Used by NESAP (NERSC KNL application readiness project) to characterize apps on Cori…



MEASURING ARITHMETIC INTENSITY

Arithmetic intensity is a measure of floating-point operations (FLOPs) performed by a given code (or code section) relative to the amount of memory accesses (Bytes) that are required to support those operations. It is most often defined as a FLOP per Byte ratio (F/B). This application note provides a methodology for determining arithmetic intensity using Intel's Software Development Emulator Toolkit (SDE) and VTune Amplifier (VTune) tools. A tutorial on using SDE on Edison can be found here, and a tutorial on using VTune can be found here. This method can also be used to determine arithmetic intensity for use in the Roofline Performance Model.

Historically, processor manufacturers have provided counters for FLOPs and/or Bytes and profiling tools to support the F/B calculation. Some modern processors such as Intel's Ivy Bridge (used in Edison) and Haswell (used in Cori Phase 1) do not provide counters for FLOPs. However, Intel's SDE can be used to count floating-point instructions in addition to core-level memory accesses, and VTune can be used to count data accesses to the uncore (off-chip DRAM DIMMs).

The SDE dynamic instruction tracing capability, and in particular the mix histogram tool, captures dynamic instructions executed, instruction length, instruction category and ISA extension grouping. Intel has developed a methodology for calculating FLOPs with SDE. In general the following uses the method "Instructions to Count Unmasked FLOP" from Intel, which is applicable for Edison and Cori Phase 1.

This application note provides additional instruction on how to only capture traces around certain key segments of a code. This is critical for real applications as both SDE and VTune collect traces that can use large amounts of disk space if tracing is enabled for more than a few minutes. And maybe more importantly, post-processing the traces can take an intractable amount of time.

An example command line for SDE is:

```
$ srun -n 4 -c 6 sde -ivb -d -iform 1 -omix my_mix.out -i -global_region -start_ssc_mark 111:repeat -stop_ssc_mark 222:repeat -
```

- Where:
- -ivb is used to target Edison's Ivy Bridge ISA (use -hsw for Cori's Haswell processors)
- -d specifies to only collect dynamic profile information
- -iform 1 turns on compute ISA iform mix
- -omix specifies the output file (and turns on -mix)
- -i specifies that each process will have a unique file name based on process ID (needed for MPI)
- -global_region will include any threads spawned by a process (needed for OpenMP)

An example command line for VTune is:

http://www.nersc.gov/users/application-performance/measuring-arithmetic-intensity/

NERSC is LBL's production computing division
CRD is LBL's Computational Research Division
NESAP is NERSC's KNL application readiness project
LBL is part of SUPER (DOE SciDAC3 Computer Science Institute)

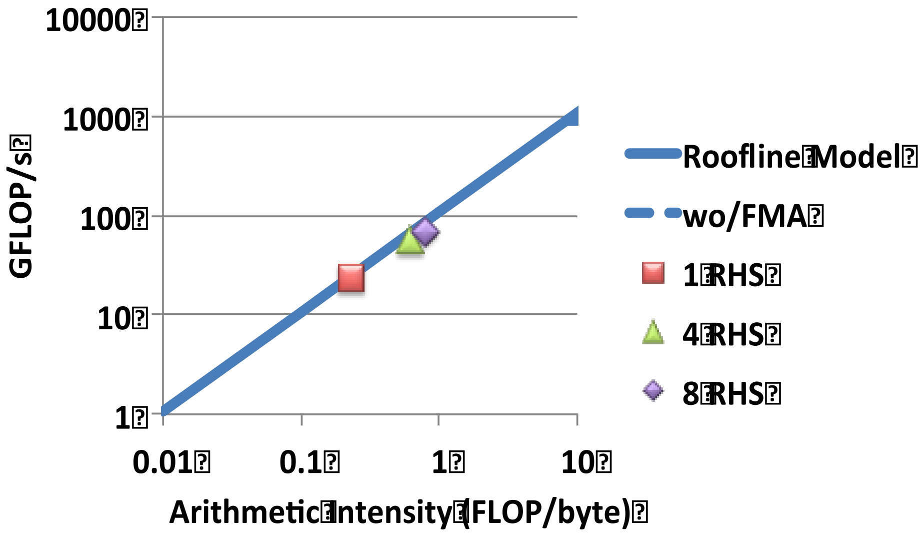
Initial Roofline Analysis of NESAP Codes

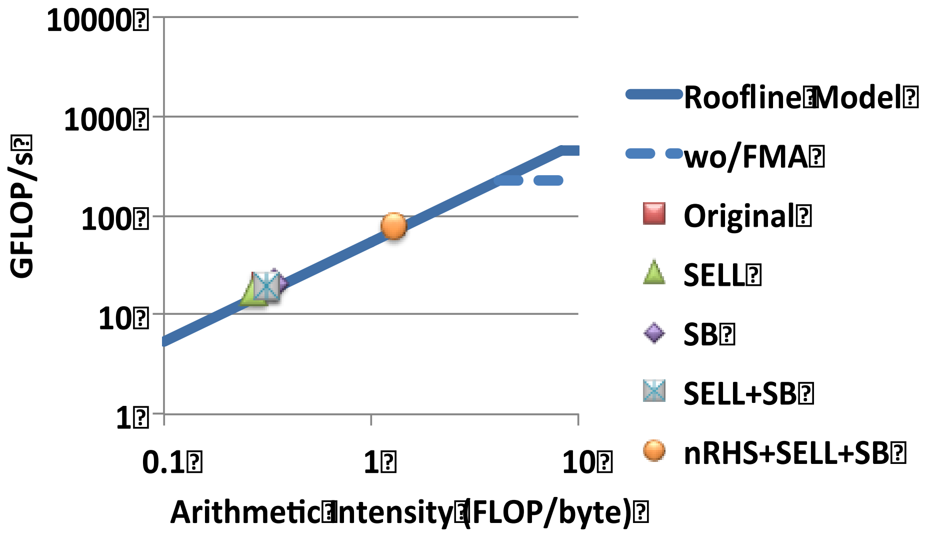
MFDn

EMGeo

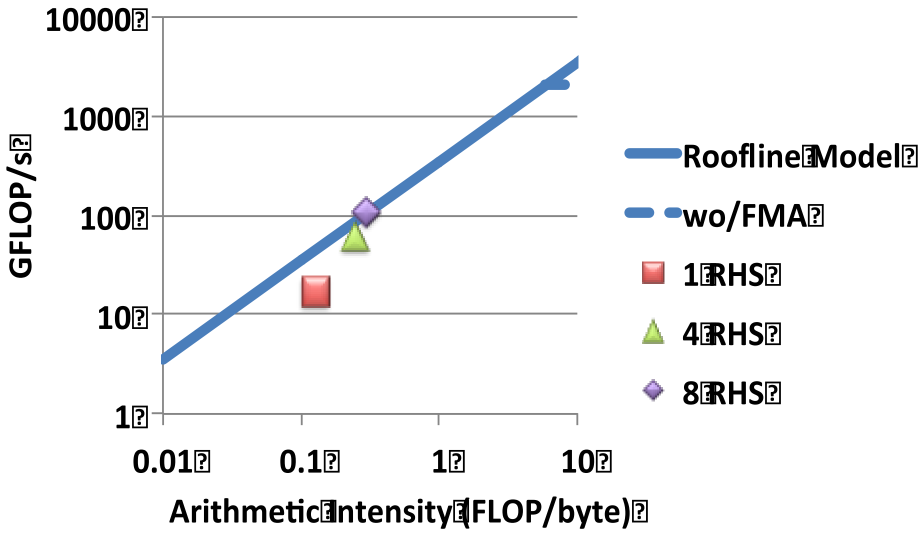
PICSAR

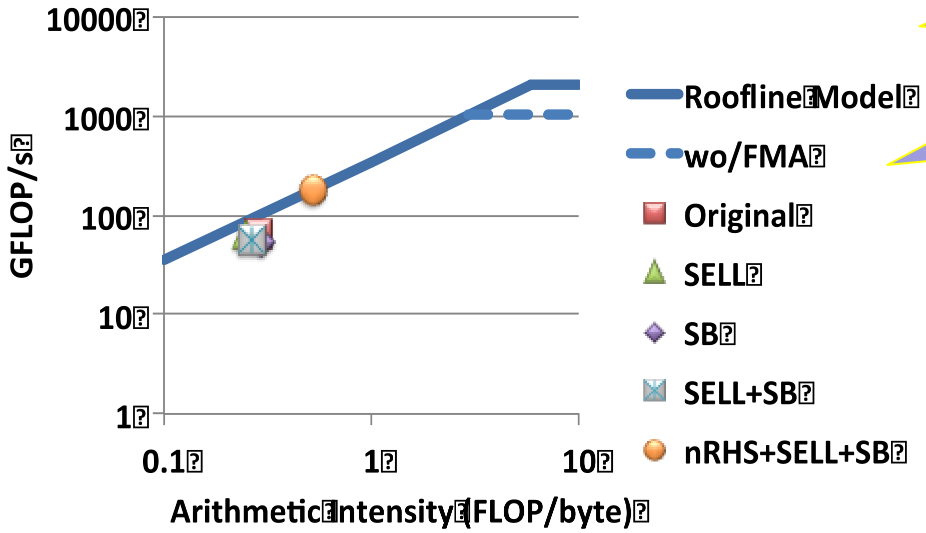
2P HSW

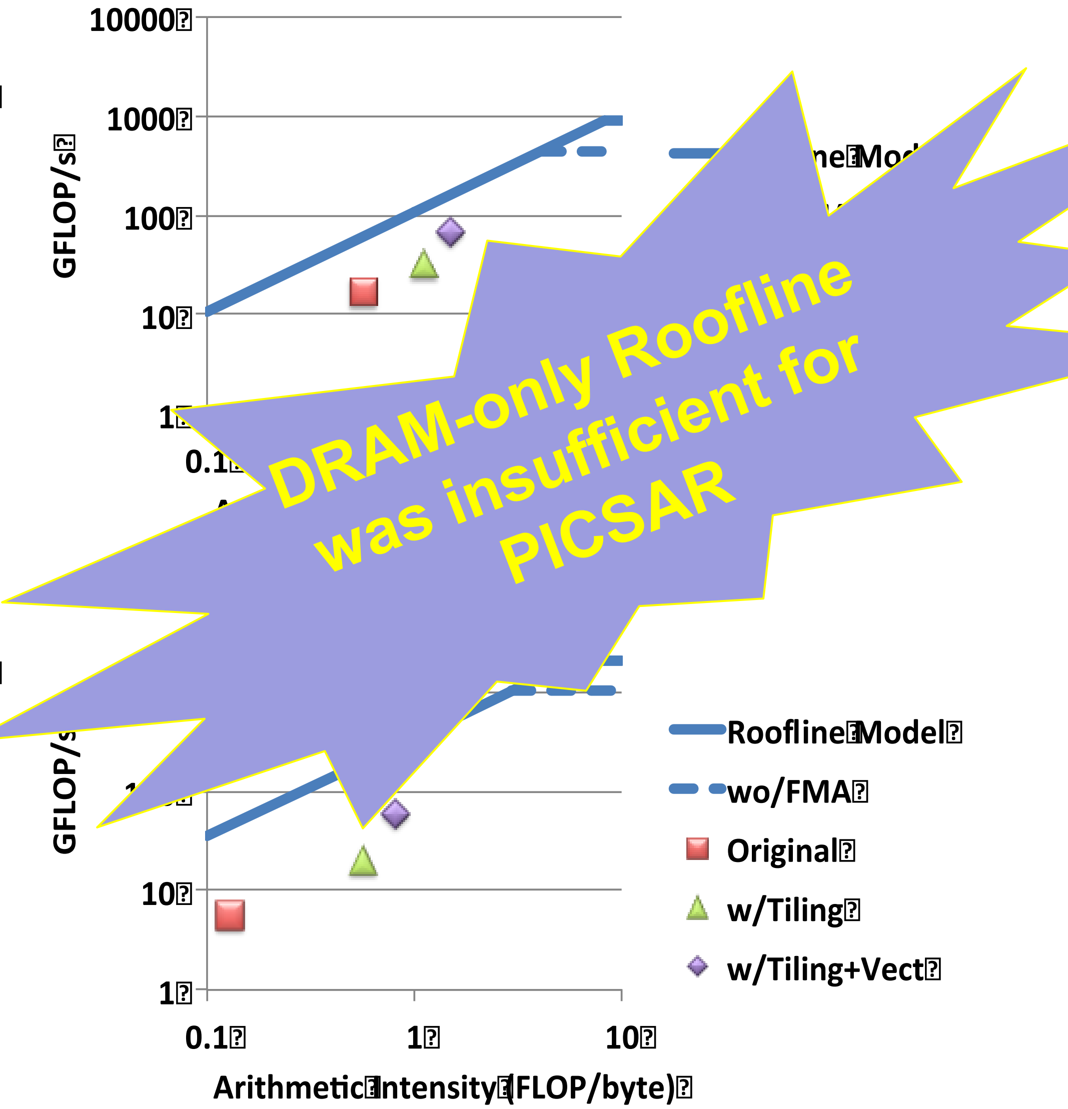




KNL







DRAM-only Roofline was insufficient for PICSAR

Nuclear physics

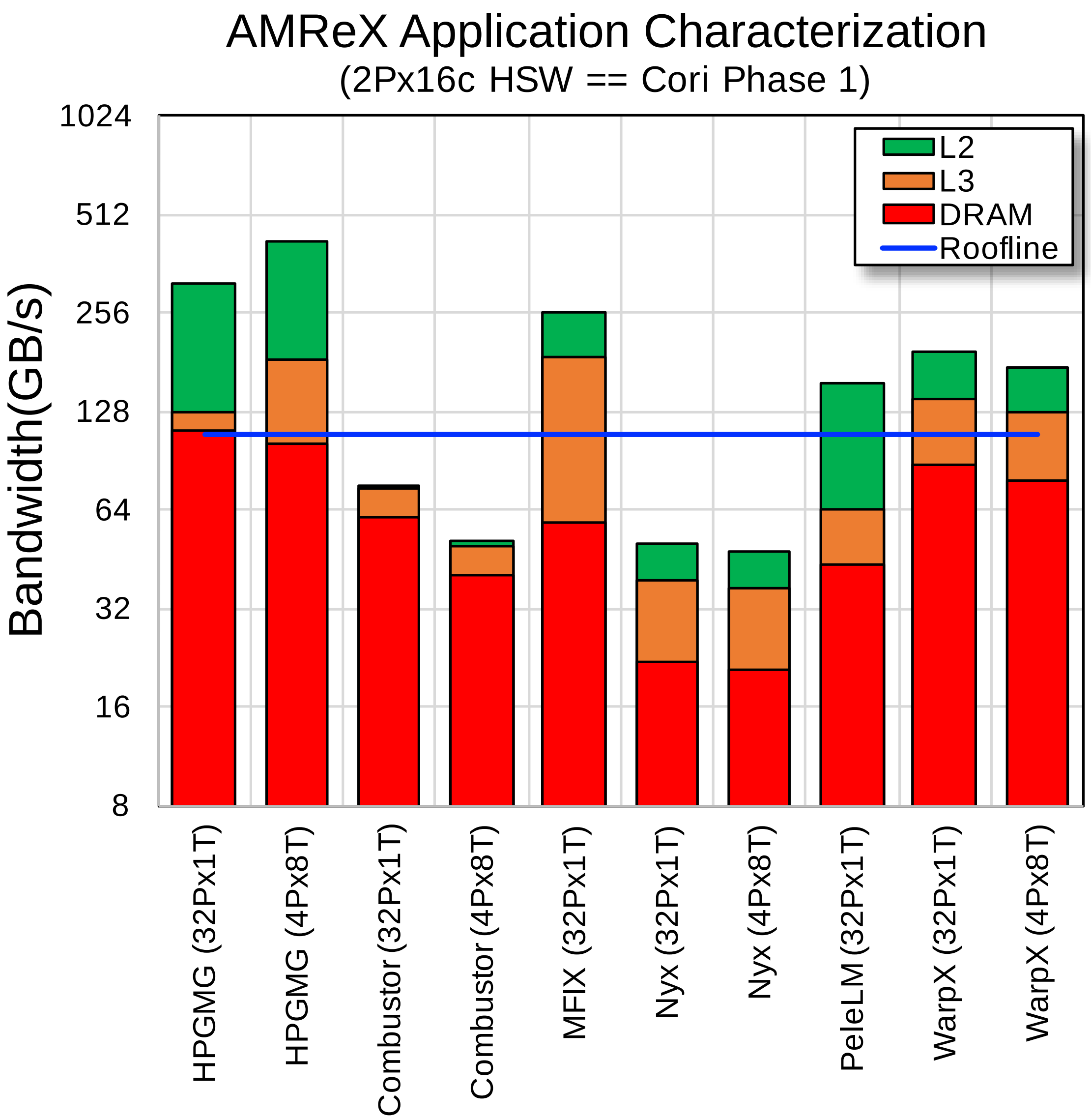
Geophysical imaging

Particle/laser interaction

Evaluation of LIKWID

- LIKWID provides easy to use wrappers for measuring performance counters…
  - ✓ **Works on NERSC production systems**
  - ✓ Minimal overhead (<1%)
  - ✓ Scalable in distributed memory (MPI-friendly)
  - ✓ Fast, high-level characterization
  - x **No detailed timing breakdown or optimization advice**
  - x **Limited by quality of hardware performance counter implementation (garbage in/garbage out)**

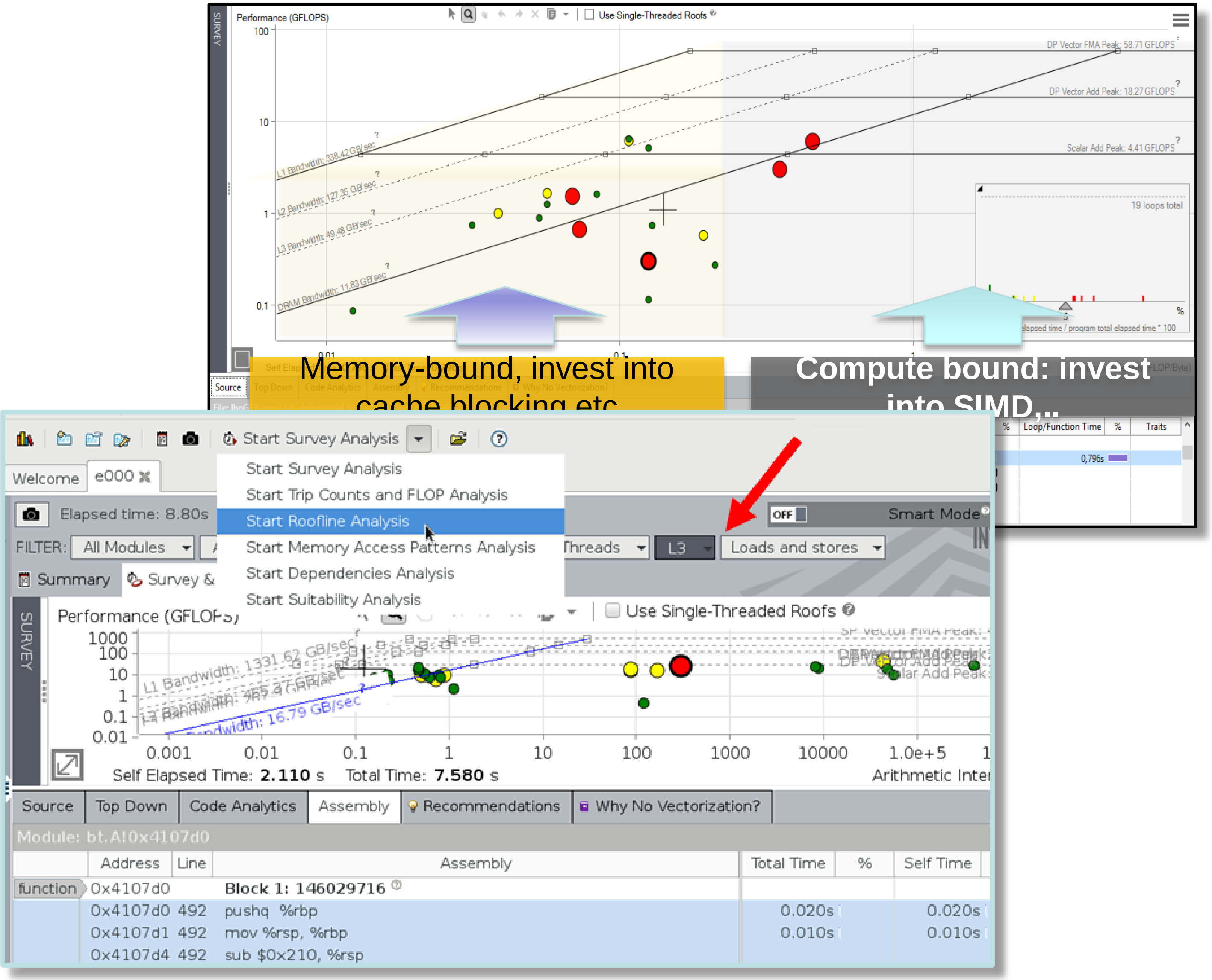
➢ **Useful tool that complements other tools**



https://github.com/RRZE-HPC/likwid

Intel Advisor

- Includes Roofline Automation…
  - ✓ Automatically instruments applications (one dot per loop nest/function)
  - ✓ Computes FLOPS and AI for each function
  - ✓ AVX-512 support that incorporates masks
  - ✓ **Integrated Cache Simulator[1] (hierarchical roofline / multiple AI's)**
  - ✓ Automatically benchmarks target system (calculates ceilings)
  - ✓ Full integration with existing Advisor capabilities


Performance (GFLOPS)
Use Single-Threaded Roofs
DP Vector FMA Peak: 58.71 GFLOPS
DP Vector Add Peak: 18.27 GFLOPS
Scalar Add Peak: 4.41 GFLOPS
L1 Bandwidth: 308.42 GB/sec
L2 Bandwidth: 127.35 GB/sec
L3 Bandwidth: 49.48 GB/sec
DRAM Bandwidth: 11.83 GB/sec
19 loops total
Start Survey Analysis
Start Trip Counts and FLOP Analysis
Start Roofline Analysis
Start Memory Access Patterns Analysis
Start Dependencies Analysis
Start Suitability Analysis
Welcome
e000
Elapsed time: 8.80s
FILTER: All Modules
Threads
L3
Loads and stores
OFF
Smart Mode
Summary
Survey &
SURVEY
Performance (GFLOPS)
1000
100
10
1
0.1
0.01
L1 Bandwidth: 1331.62 GB/sec
L3 Bandwidth: 16.79 GB/sec
0.001
0.01
0.1
1
10
100
1000
10000
1.0e+5
Arithmetic Inter
Self Elapsed Time: 2.110 s
Total Time: 7.580 s
Source
Top Down
Code Analytics
Assembly
Recommendations
Why No Vectorization?
Module: bt.A!0x4107d0

Memory-bound, invest into cache blocking etc

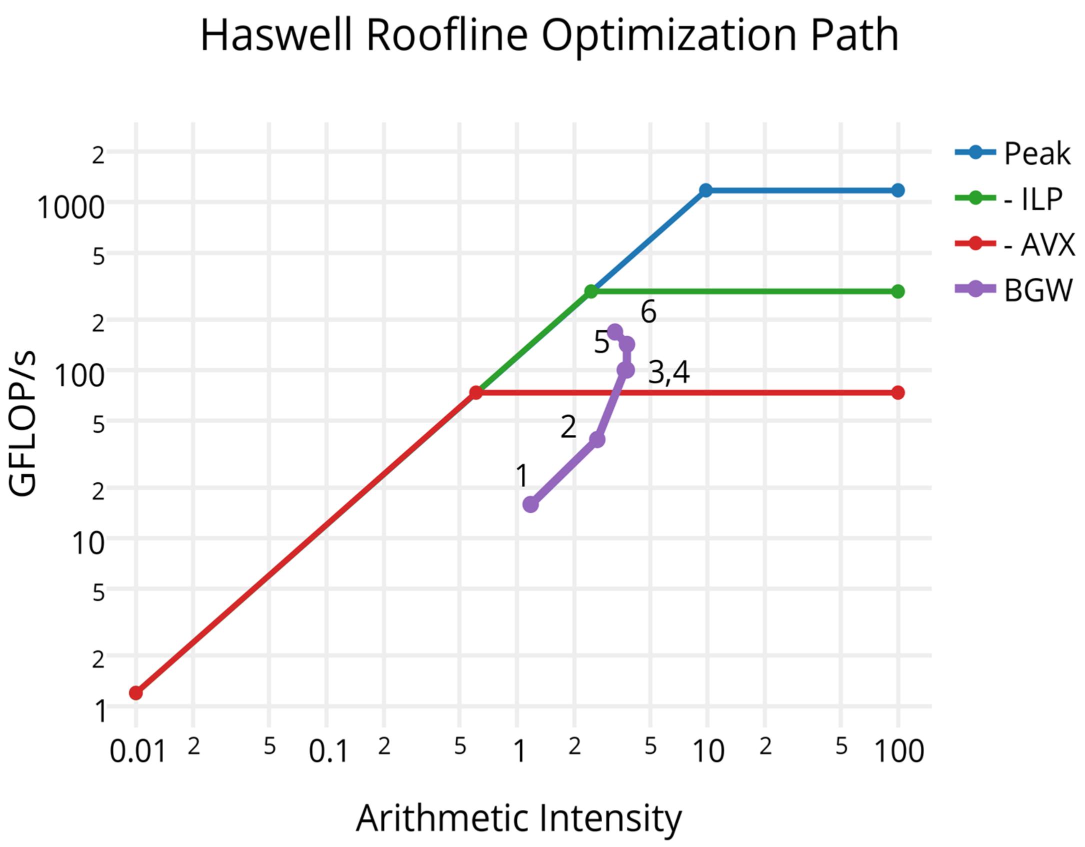
Compute bound: invest into SIMD,..

	Address	Line	Assembly	Total Time	%	Self Time
function	0x4107d0		Block 1: 146029716			
	0x4107d0	492	pushq %rbp	0.020s		0.020s
	0x4107d1	492	mov %rsp, %rbp	0.010s		0.010s
	0x4107d4	492	sub $0x210, %rsp			

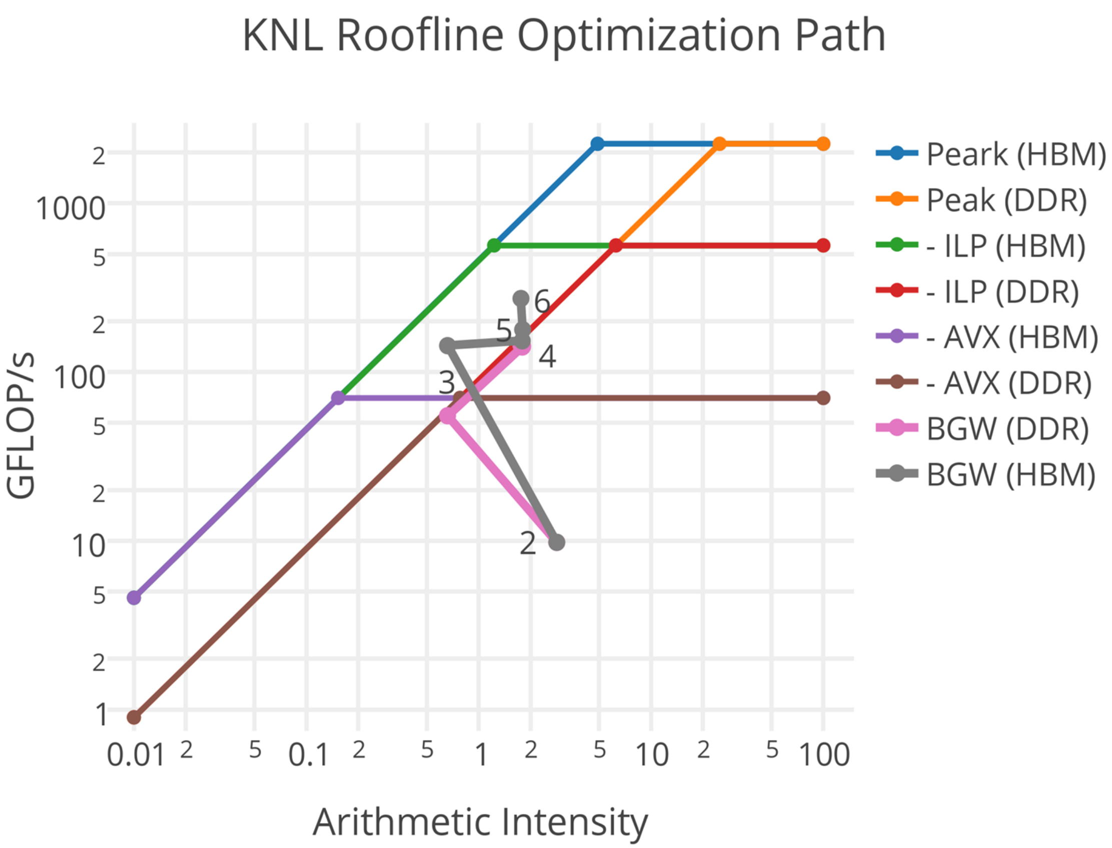
http://www.nersc.gov/users/training/events/roofline-training-1182017-1192017

[1] Technology Preview, not in official product roadmap so far.

Tracking Optimization Behavior



Haswell Roofline Optimization Path



KNL Roofline Optimization Path

BerkeleyGW: Optimization process for Kernel-C (Sigma code):

1. Refactor (3 Loops for MPI, OpenMP, Vectors)
2. Add OpenMP
3. Initial Vectorization (loop reordering, conditional removal)
4. Cache-Blocking
5. Improved Vectorization (Divides)
6. Hyper-threading

BerkeleyGW is a material science application that is dominated by dense linear algebra, including distributed matrix multiplication, inversion, diagonalization, and contraction and fast fourier transforms (FFT).

Acknowledgements

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